UNIVERSITY AT STONY BROOK

CEAS Technical Report 753

GROUND BOUNCE EFFECTS IN DIELECTRIC AND SUBSTRATE COUPLING BETWEEN IC INTERCONNECTS

Armen H. Zemanian and Tao Li

This work was supported by the National Science Foundation under Grant MIP-9423732.

January 7, 1998

bounce" should not be ignored even in that case. It does this by first indicating through a very simple lumped model how substrate resistance in conjunction with capacitance coupling actually increases the transient coupling between interconnects — as compared to the conventional purely capacitive model. It then examines a more realistic model, wherein the fringing electric field in both the dielectric and the resistive substrate are more accurately analyzed through a finite difference analysis. The fringing electric field leads to an exterior problem requiring an infinite electrical network analysis. Recent results regarding such infinite models are used to reduce the numerical computations. All this simulation shows that the transient interference as determined by our more accurate model is much more severe than that indicated by the simplified lumped model. In short, distributed substrate resistance must be included along with the capacitance coupling in order to fully account for the digital-to-analog interference in IC interconnects.

In order to make our point briefly and simply, we restrict our models to two-dimensional configurations with linear media. Nonetheless, this analysis can be directly extended to three-dimensional models at the expense of much larger numerical computations. Furthermore, nonuniform doping in the substrate and nonlinear capacitances of depletion regions within the semiconductor will also complicate the model, but our general conclusion regarding the importance of incorporating substrate resistance for interconnect cross-talk should remain valid.

2 Lumped Models

A clue as to the importance of substrate resistance in the case of electric-field coupling between interconnects can be readily obtained by examining two simple lumped models. In Fig. 1(a) a digital interconnect with a unit step of voltage $u(t)$ is adjacent to an analog interconnect with a voltage $v(t)$ induced through three 1 F coupling capacitors, as shown. (For the sake of numerical simplicity we normalize parameter values to unit values.) The semiconductor is taken to be at ground potential. The result is that $v(t) = .5$ V for all $t > 0$.

Now, let us more realistically but still very simplistically model the semiconductor substrate by three 1 Ω resistors, two of which connect to the grounded back plate of the semiconductor chip. See Fig. 1(b). The final value of the induced voltage $v(t)$ is again .5 V, but its earlier voltages are substantially stronger, starting off at 1 V and then dropping to .5 V. This is due to the "ground bounce" of the semiconductor under the analog interconnect, which is (simplistically) represented by the voltage $v_2(t)$. That too starts off at 1 V but then decays to zero. Thus, it appears to be important to take into account ground bounce when designing digital and analog VLSI interconnects, but a still more realistic model should be examined in order to verify this inference.

3 A Distributed Model

More accurate results can be obtained from a finite-difference analysis of the electric fields in the dielectric surrounding the interconnects and in the substrate. That analysis can be implemented by a capacitive grid representing the dielectric and a resistive grid representing the substrate semiconductor. The layout is shown in Fig. 2. The infinite line through C and D represents the surface between the dielectric and the semiconductor. So as to include the fringing of the electric field, the capacitive grid extends infinitely to the left and right (above the line through A and B) and infinitely upwards, and the resistive grid extends infinitely to the left and right and infinitely downwards (since the substrate is much thicker than the dimensions of the interconnects). Again for the sake of numerical simplicity we normalize all incremental capacitor and resistor values in those grids to 1 F and 1 Ω respectively. This only changes the time constant of the voltage variation on the analog interconnect but does not change its shape. Moreover, by using infinite grids as stated, we avoid the medium-truncation errors arising in conventional finite-difference analyses of exterior problems.

We can use the theory of infinite electrical networks [8, Chapter 7] to analyze this model. Let us briefly summarize the steps of that analysis. The infinite capacitive grid above the line through A and B in Fig. 2 can be replaced by an infinite set of terminating capacitors, one capacitor between each pair of nodes on that line. These terminating capacitors affect the discretized electric field below that line in exactly the same way as does the discretized medium above that line. Similarly, the infinite resistive grid can be represented perfectly accurately by an infinite set of terminating resistors, one resistor between each pair of nodes along the line through C and D in Fig. 2. All this yields an infinite RC network for the region between the lines through AB and CD (including the terminating elements). As the next step, we now incur some truncation error by terminating the latter network by grounding the regions to the left of AD and to the right of BC. The resulting truncation error is very much smaller than that incurred in the usual finite-difference analysis that employs a truncation along a finite perimeter that encloses the model on all sides [6], [8, Section 8.2]. This yields finally a finite RC network which can be analyzed for the transient voltage $v(t)$ on the analog interconnect induced by a unit step of voltage $u(t)$ imposed upon the digital interconnect.

Accordingly, we computed the Laplace transform $V(s)$ of $v(t)$ for various real values of s and then used the Gaver-Stehfest algorithm [5] to get $v(t)$. The result is shown in Fig. 3. The final value 0.1171 V of $v(t)$ is the value of voltage induced on the analog interconnect in the case where the substrate is treated as a perfect conductor, that is, it is the value induced only by capacitive coupling. It is most significant that, although that final value of $v(t)$ is much smaller than the 1 V

jump in voltage on the digital interconnect, the initial jump in v(t), about 0.48 V, is much more significant. A purely capacitive model, wherein the substrate is treated as a perfect conductor, would only indicate that final value 0.1171 V as the amount of voltage interference induced on the analog interconnect by a 1 V jump on the digital interconnect. However, our present model, wherein the resistance of the substrate is taken into account, indicates that there is a much greater interference initially induced.

We also computed the voltage transient at two points on the semiconductor surface directly under the centers of the digital and analog wires, to get an indication of the ground bounce. Under the digital wire, the ground-bounce voltage starts at 0.8848 V at $t = 0.1$ sec. (as compared to 0.4764 V for the analog wire) and then decays to 0 V, crossing the analog-wire transient at 5.6 sec. Under the analog-wire, the ground-bounce voltage starts at 0.4905 V at $t = 0.1$ sec. and then decays to 0 V, crossing the analog-wire transient at $t = 0.5$ sec. Thus, the surface of the semiconductor experiences an initial substantial jump in voltage with respect to ground, which in this model is at infinity. As was mentioned above, ground-at-infinity is reasonable since the chip's thickness is very much greater than the dimensions of the interconnects. Nonetheless, finite semiconductor depth can also be taken into account by using the analysis of layered media given in [8, Chapter 7].

4 Conclusion

We conclude that it is essential that the substrate resistance be included in any analysis of crosstalk from digital to analog interconnects. A purely capacitive analysis will entirely miss the initial severe interference. To be sure, our present resistance-capacitance model is still rather simplistic, being only two-dimensional and linear. More accurate simulations with three-dimensional models with nonlinear parameters are called for. Nonetheless, this brief paper does point out the need for incorporating ground bounce in cross-talk analyses between interconnects. This is in addition to ground bounce effects on devices.

References

[1] J.A. DeFalco, Put a damper on ground bounce, *Electronic Design*, August, 1993, pp. 71-79.

[2] B. Nauta and G. Hoogzaad, How to deal with substrate noise in analog CMOS circuits?, *Proc. 1997 European Conference on Circuit Theory and Design*, Budapest, September 1997.

[3] D.K. Su, M.J. Loinaz, S. Masui, and B.A. Wooley, Experimental results and modeling techniques for substrate noise in mixed-signal integrated circuits, *IEEE J. Solid-State Circuits* vol. 28, April 1993, pp. 420-429.

[4] D. Wouter, J. Groeneveld, and D.T. de Jong, Groundbounce in CMOS, *Analog Circuit Design*, W. Sansone et al (eds.), 1994, pp. 3-22.

[5] H. Stehfest, Algorithm for numerical inversion of Laplace transforms, *Communicat. Assoc. Computing Machinery*, vol. 13, pp. 47-49, 624, 1970.

[6] A.H. Zemanian, A finite-difference procedure for the exterior problem inherent in capacitance computations for VLSI interconnections, *IEEE Trans. Electron Devices*, vol. 35, pp. 985-992, 1988.

[7] A.H. Zemanian, R.P. Tewarson, C.P. Ju, J.F. Jen, Three-dimensional capacitance computations for VLSI/ULSI interconnections, *IEEE Trans. on Computer-Aided Design*, vol. 8, pp. 1319-1326, December, 1989.

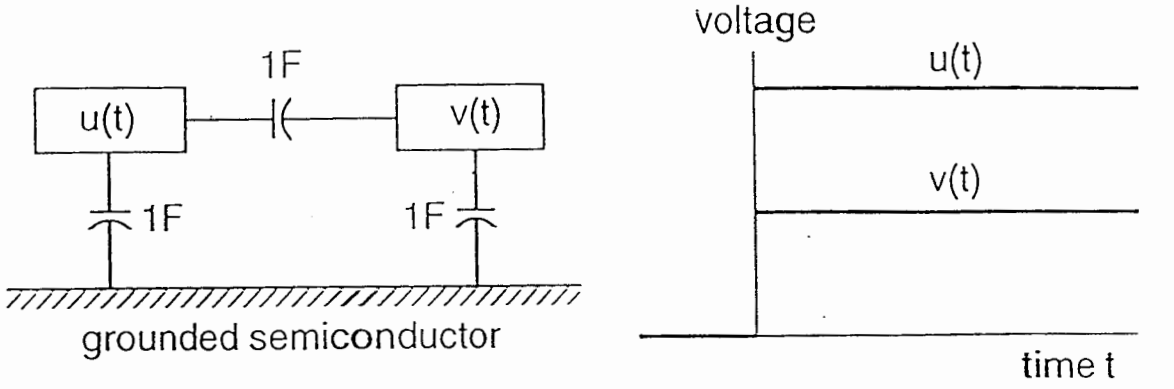
[8] A.H. Zemanian, *Infinite Electrical Networks*, Cambridge University Press, New York, 1991.

Figure Captions

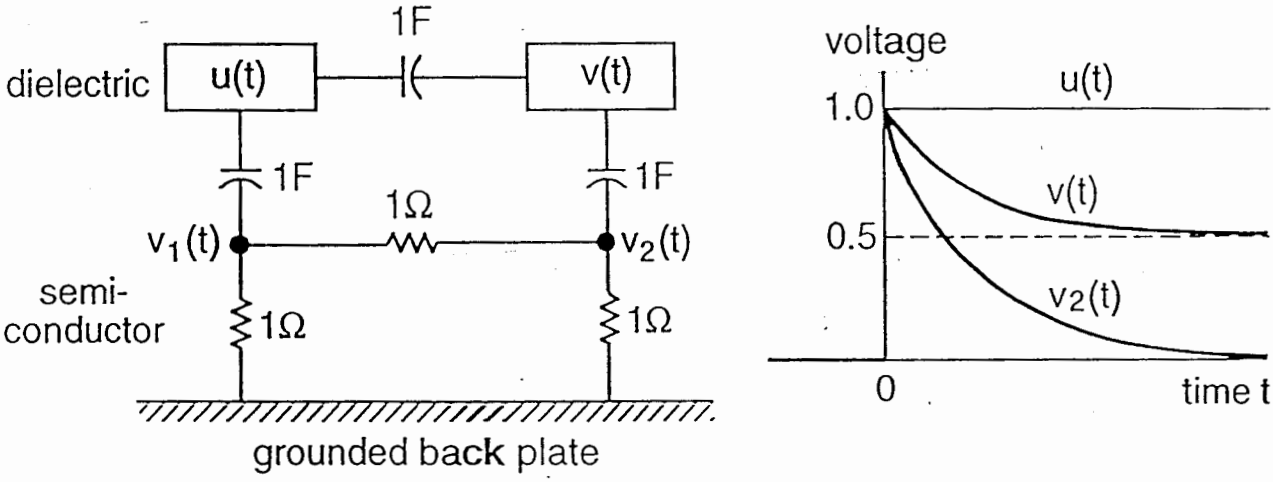
Fig. 1. (a) The purely capacitive lumped model. (b) The lumped model with capacitors for the dielectric and resistors for the semiconductor.

Fig. 2. The layout for the finite-difference computation.

Fig. 3. The voltage transient on the analog wire induced by a 1 V jump on the digital wire.


1F
u(t)
v(t)
1F
1F
grounded semiconductor
voltage
u(t)
v(t)
time t

(a)


1F
dielectric
u(t)
v(t)
1F
1F
1Ω
$v_1(t)$
$v_2(t)$
semi-
conductor
1Ω
1Ω
grounded back plate
voltage
u(t)
1.0
v(t)
0.5
$v_2(t)$
0
time t

(b)

Fig. 1

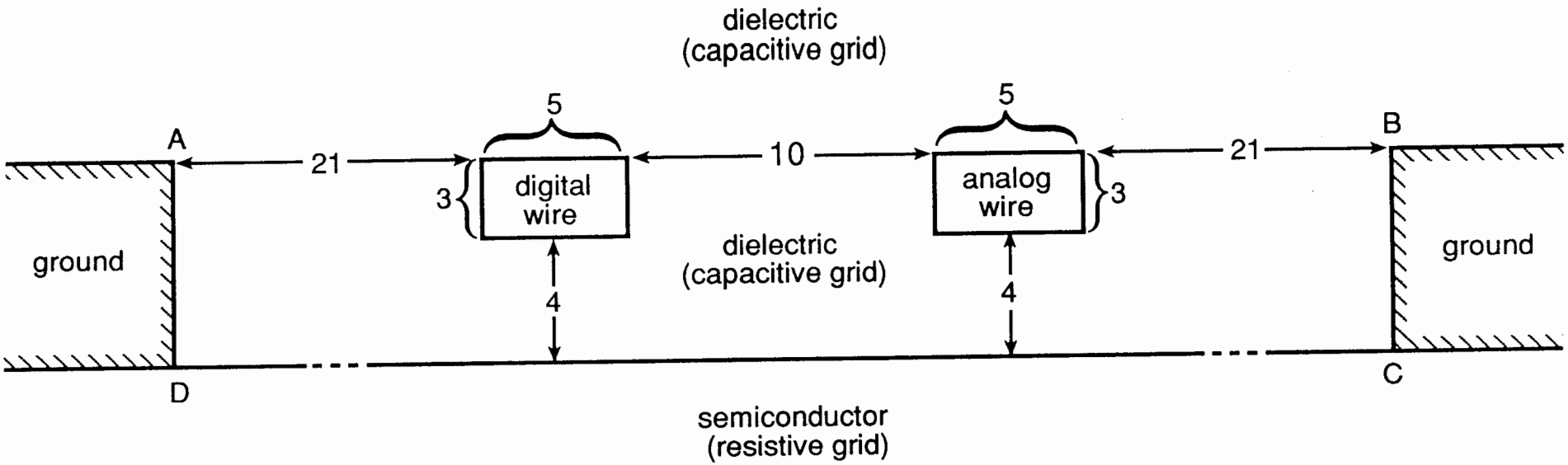

dielectric
(capacitive grid)
5
5
A
B
21
10
21
3
digital
wire
analog
wire
3
ground
dielectric
(capacitive grid)
ground
4
4
D
C
semiconductor
(resistive grid)

Fig. 2

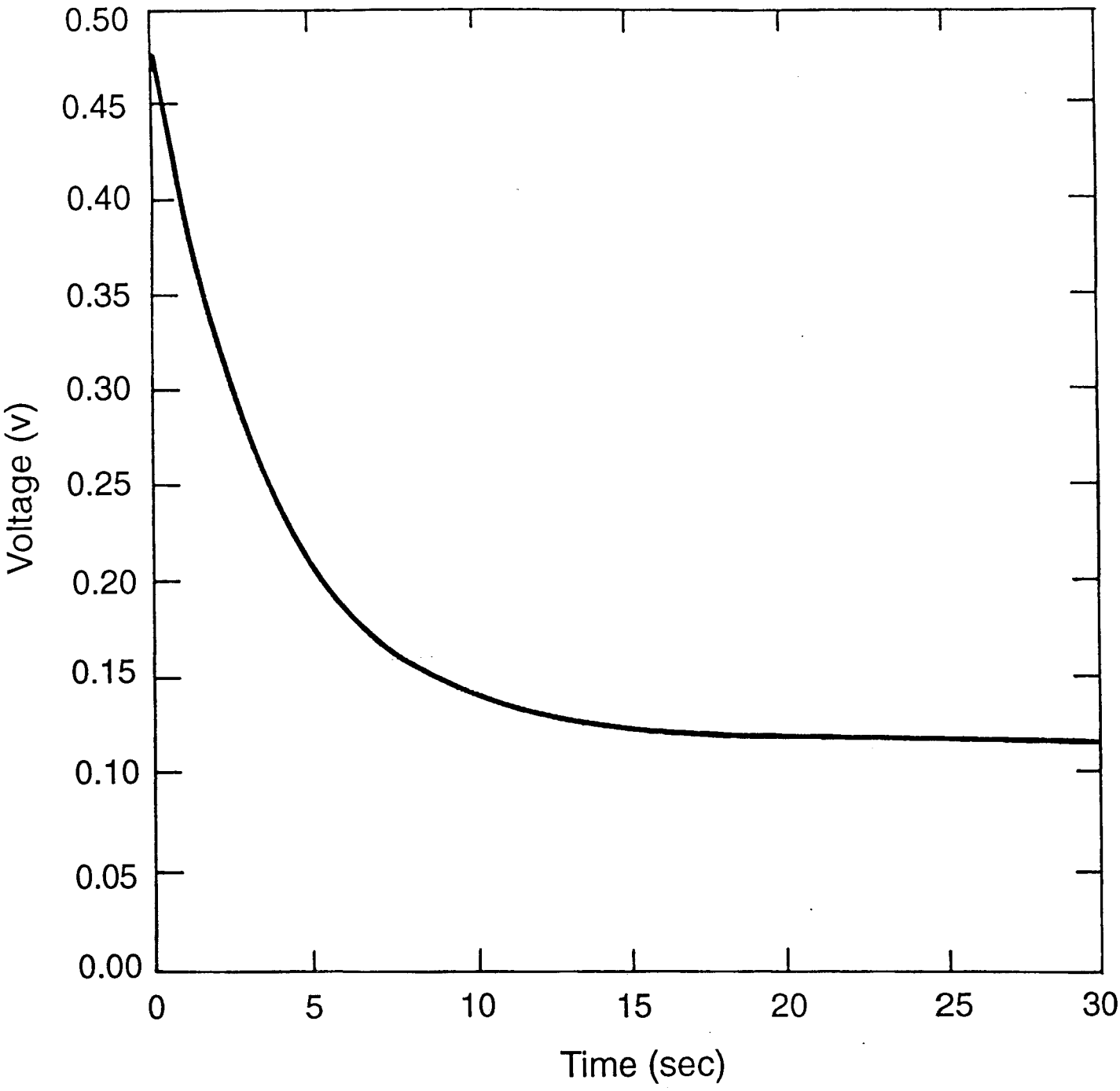

0.50
0.45
0.40
0.35
0.30
0.25
0.20
0.15
0.10
0.05
0.00
Voltage (v)
0
5
10
15
20
25
30
Time (sec)

Fig. 3