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EXTERIOR TEMPLATES FOR CAPACITANCE COMPUTATIONS

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# EXTERIOR TEMPLATES FOR CAPACITANCE COMPUTATIONS \*

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**Abstract** — The computation of the capacitance coefficients for alternative interconnect configurations requiring repeated calculations as the configurations are changed can be substantially accelerated by using an “exterior template,” that is, a set of “template capacitors” connected to the surface of the smallest rectangular region encompassing the planned interconnects. These template capacitors represent the effect of the medium for the fringing field outside the rectangle, and they eliminate the need to sample the fringing field every time a new calculation is made. The template capacitors can be determined by using the theory of infinite grids to eliminate almost entirely the medium-truncation error. All this works for both two-dimensional and three-dimensional configurations, and it is especially advantageous in the three-dimensional case.

*Key Words:* Capacitance computations, alternative interconnect configurations, template capacitors, infinite grids.

## 1 Introduction

Sufficiently accurate determinations of capacitance coefficients for wiring in VLSI circuit designs remain a continuing problem, despite the fact that much effort has been directed toward resolving it for quite a few years. Fairly extensive, but by no means complete, references to such efforts can be found in the bibliographies of references [1] through [12]. This persistent difficulty arises at least partially from the facts that capacitance computations must take into account the fringing of the electric fields because that fringing contributes substantially to the capacitance values, and on the other hand that fringing extends far beyond the restricted regions between the wires and the semiconductor chip's surface. Thus,

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accurate determination of capacitances will perforce require a finite-difference or finite-element analysis with a large number of sampling points, most of which lie far outside the regions where the wiring occurs. Alternatively, a Green's function approach might be used; but, the Green's functions must in general account for multilevel semi-infinite media wherein the fringing takes place and thereby become complicated functions requiring numerical integration over the surfaces of the conductors.<sup>1</sup> All this strains both computer-memory requirements and computation time, especially if a sufficiently fine array of sampling nodes is chosen to have any hope of an accurate computation, and similarly for the surface elements in the Green's function approach. The problem is especially severe for a three-dimensional multiwire configuration, which after all is what often arises in practical design problems. One can mitigate to some extent this fringing-field problem by using a nonuniform sampling array, which is dense between the wires and which becomes progressively sparser as distance from the wires increases; the problem may be somewhat eased in this way but by no means eliminated. The various tools presently available for determining capacitance coefficients reflect this problem by yielding insufficiently accurate results in many cases.

The purpose of this short paper is to suggest augmenting the finite-difference technique with a procedure that will make it still more competitive with the many other extant methods of capacitance evaluation. Currently, there is no "best method" for the computation of capacitances, and our suggestion will not alter that fact. Our goal is to propose an additional procedure that may at times enhance the finite-difference approach.

More specifically, we present a computational technique that will entirely eliminate the need to sample the fringing field every time a capacitance computation is repeated. The idea is to choose the smallest two-dimensional or three-dimensional rectangular region (let's call it a "box") that contains all the wiring whose capacitance coefficients are desired and then to determine a set of "template capacitors" connected to the sampling nodes on the surface of the box; those template capacitors will represent the surrounding medium wherein the fringing takes place. This initial computation of the template capacitors also faces the same difficulty of large memory and computation-time requirements as do the conventional

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<sup>1</sup>Still another approach is to derive approximate analytical formulas for capacitances, but these are generally less accurate and of restricted usage.

techniques, but once the template capacitors are determined they will not change as the wiring configuration within the box is altered in any arbitrary fashion. The set of template capacitors connected to the surface of the box will be called an "exterior template."

In short, given a medium exterior to the box and a determination of the corresponding exterior template, an engineer can try various wiring designs without having to sample the exterior medium. The computation of capacitance coefficients for each new design will only involve the very much smaller set of sampling nodes within the box.

## 2 The Exterior Template

Even though a determination of an exterior template need be done only once and for all of the possible wiring layouts within the box, given the exterior medium and the choice of sampling points on and outside the box, the fact remains that the computation of the template capacitors remains an onerous task requiring much computer memory and time. However, certain steps can be taken to reduce that task.

For the sake of a simpler exposition, let us describe those steps for the two-dimensional case. Everything we will say extends directly to the three-dimensional case. Consider the configuration shown in Fig. 1. We have several interconnection wires lying above a ground plane that represents the surface of a semiconductor chip. We wish to determine the self and mutual capacitances of those interconnects. A conventional finite-difference analysis that is acceptably accurate would require an analysis of a discretization of Laplace's equation in a region sufficiently large to account for almost all of the fringing of the electric field, as for example the region within the large rectangle  $ABCD$  shown in Fig. 2. The discretization is implemented through the choice of sampling points distributed throughout the interior of  $ABCD$ . The boundary of  $ABCD$  is taken to be at 0 volt so as to represent approximately the zero potential at infinity.<sup>2</sup> This induces a medium-truncation error. It also requires many sampling points and an onerous numerical computation. Worse yet, this difficulty is repeated in its entirety every time a new configuration of interconnects with perhaps a different number of them is planned.

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<sup>2</sup>Some prefer to use a Neumann condition along the boundary; this is in effect an open circuit along that boundary for the capacitive grid representing the field.

To avoid this problem, we propose a multidimensional version of the idea of a driving-point capacitance to represent all of the medium outside the smallest box that encompasses all the interconnects. That box is shown in Figs. 1 and 3 as the smaller rectangle  $abcd$ . We choose a set of sampling points (call them “template nodes”) along that box’s perimeter. Those points have to be equally spaced along the upper side of the box, and similarly along the lower side; however, the upper increments may be different from the lower increments. (In our figures, we have shown all increments as being the same.) We wish to determine a set of “template capacitors” from each template node to every other template node that will serve to represent the discretized medium (including the ground plane) outside the box. For example, if there are  $k$  template nodes, then from each template node, say,  $n_0$  there will be  $k - 1$  template capacitors connected from  $n_0$  to all the other template nodes — and in addition a template capacitor from  $n_0$  to ground, which reflects the presence of the ground plane. Just a few of those capacitors are indicated in Fig. 3. For  $k$  template nodes there will be altogether  $(k + 1)k/2$  template capacitors.

### 3 Determining the Template Capacitors

The template capacitors connected from any template node  $n_0$  to all the other template nodes can be determined by assuming that every template node is a very small conductor with  $n_0$  at 1 volt and all the other template nodes at 0 volt. Furthermore, the discretization of the medium outside the box  $abcd$  yields a grid of incremental capacitors.<sup>3</sup> Since the medium occupies the infinite half-space above the ground plane, we are faced with analyzing an infinite capacitive grid. We wish to avoid as much as possible the medium truncation indicated in Fig. 2, for that introduces an unnecessary error.

Almost always, the medium above the semiconductor chip can be taken to be horizontally layered, consisting of a dielectric layer and then air above it or perhaps several dielectric layers and then air. This configuration allows us to exploit the theory of infinite electrical grids to obtain a far more rapid means of determining the template capacitors and moreover avoiding almost all of the truncation error that the truncation of Fig. 2 would

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<sup>3</sup>The standard formulas for the incremental capacitors can be found in [11] and [12] for the two-dimensional and three-dimensional cases respectively.

induce. Two steps are involved.

In the first step, all of the discretized medium above the two-way infinite horizontal line through  $b$  and  $c$  in Fig. 3 can be analyzed according to [11, Section III] (see also [13, Example 8.2-1]) to obtain an infinite set of "terminating capacitors" connecting each node on that line to all the other nodes on that line. This is illustrated in Fig. 4, which shows just six of those terminating capacitors at a node on that line. Because of the horizontal layering above that line, the upper terminating capacitors incident to any node are the same as those incident to any other node on that upper line. Moreover, the values of the terminating capacitors can be obtained very rapidly indeed by using the fast Fourier transform on formulas derived from the theory of infinite grids. These terminating capacitors represent the infinite discretized medium above the said line exactly — there is no truncation error at this point.<sup>4</sup>

In a similar fashion, the discretized medium between the two-way infinite line through points  $a$  and  $d$  and the ground line can be represented exactly by terminating capacitors at the nodes along line through  $a$  and  $d$ . This is indicated by just seven terminating capacitors at one such node. In this case there is in addition a terminating capacitor to ground; it reflects the presence of the ground line.

(In the three-dimensional case, the formulas for the terminating capacitors are given in [12, Section 3].)

The second step toward obtaining the template capacitors is to analyze the capacitive grid consisting of the incremental capacitors in the strip between the two lines through  $bc$  and  $ad$  along with the terminating capacitors. (There are no capacitors within the box because we are calculating an exterior template.) Now, however, we are obliged to truncate the strip. This is done by grounding all the nodes beyond some distance to the left and right of the box, as is indicated in Fig. 5. This truncation with grounding half-strips introduces a far smaller error than does the all-encompassing truncation of Fig. 2.<sup>5</sup> Finally, we can analyze the much smaller capacitive network indicated in Fig. 5 to get the template capacitors as follows. Choose any template node  $n_0$  and set it at 1 V. Set all other template nodes at 0 V. Write nodal equations for the unknown node voltages between the grounding half-strips

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<sup>4</sup>However, the discretization brings in its own error.

<sup>5</sup>This assumes the same distances to the truncations in Figs. 2 and 5 leftward and rightward.

and the box.<sup>6</sup> We now solve the nodal equations to get the node voltages within the strip between the grounding half-strips and the box. These in turn determine the charges at each of the template nodes. Those charges determine the self and mutual capacitances incident to  $n_0$  (see [11, Section IV]), which in fact are the desired template capacitors incident to  $n_0$ . This procedure is repeated for each of the nodes along the box's perimeter.

It is worth noting that the sum of all the template grounding capacitors, namely, those connected from ground to the template nodes, is equal to the total self capacitance of a single conductor occupying all of the box. Thus, a conductor that is 20 units wide, 4 units thick, and 8 units above the ground plane in a dielectric of unit permittivity was found to have a capacitance of 5.4174 farads by this method. This value agrees with the value 5.42 found in [11, Example 1].

## 4 Conclusions

We have pointed out a fast procedure for determining the template capacitors for a rectangular region within a layered medium above a ground plane. With the template capacitors in hand, any configuration of conductors inside the template (i.e., inside the box) can be analyzed via a finite-difference computation restricted to the interior of the template to obtain the self and mutual capacitances of those conductors. This involves solving a capacitive grid within the box along with the template capacitors at the template nodes on the box's boundary. The capacitive grid within the box is obtained in the standard way by discretizing Laplace's equation. The resulting analysis will involve far fewer nodes than would a conventional analysis based on Figure 2. Moreover, the template approach will have a much smaller truncation error than that of a conventional analysis if the template computation is based on the theory of infinite grids as described above. To be sure, the template approach induces a full matrix whereas the conventional analysis induces a sparse one; but, the far fewer nodes for the template can more than compensate for the fullness

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<sup>6</sup>It is a fact that the sum  $C_T$  of all the terminating capacitors at any node  $n_1$  on the upper line is the "DC term" of the fast Fourier transform of the equations representing the medium above the strip [11, Section III]. So, the contribution of the infinity of terminating capacitors incident to  $n_1$  due to the voltage  $v_1$  at  $n_1$  is simply  $C_T v_1$ . Thus, there is no need to write an infinite series at this point. The same is true for any node on the lower line.

of its matrix, thereby providing a possibly substantial computational advantage. For example, if the nodes of Fig. 2 were  $n^2$  in number but those for the template along with the nodes within the box were  $p \times q$  in number, the nodal-analysis matrix for the conventional approach would be an  $n^2 \times n^2$  matrix whereas that for the template approach would be a  $(p \times q) \times (p \times q)$  matrix. For  $n = 1000$ ,  $p = 100$ , and  $q = 20$ , the first matrix would be  $10^6 \times 10^6$  in size but the second only  $2000 \times 2000$  in size.

All of this extends directly to the three-dimensional case and provides an even greater advantage there, for now we cube node numbers instead of squaring them. In fact, it is in the three-dimensional case that this use of exterior templates will be of greatest importance. Indeed, conventional finite-difference analyses of three-dimensional configurations generally lead to unacceptably large matrices, whereas the template approach can decrease the matrix sizes radically enough to make three-dimensional analyses feasible.

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## Figure Captions

- Fig. 1.** A possible set of conductors embedded in a layered dielectric above a ground plane whose self and mutual capacitances are to be determined. The "box" is the rectangular region delineated by the dashed lines with corners  $a$ ,  $b$ ,  $c$ , and  $d$ .
- Fig. 2.** The surface truncating the medium in the conventional finite-difference approach. That surface is shown by the three dashed lines connecting the points  $A$ ,  $B$ ,  $C$ , and  $D$ .
- Fig. 3.** The template capacitors connected to a particular node  $n_0$ . Only some of these are shown. There is in fact a template capacitor connected between every two template nodes, as well as a template capacitor from each template node to ground.
- Fig. 4.** The terminating capacitors at the nodes of the two-way infinite horizontal lines passing through the top and bottom of the box. Only a few of these are shown. There is a terminating capacitor between every two nodes on the upper line, and similarly for the lower line. Moreover, along the lower line there is a capacitor connecting each node to ground.
- Fig. 5.** Some of the incremental capacitors within the smallest horizontal strip containing the box and some of the terminating capacitors connected to the upper and lower surfaces of the strip. The grounding half-strips are shown cross-hatched at the left and right. At this point of the analysis, there are no capacitors within the box nor of course within the grounding half-strips.

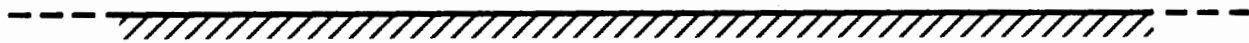
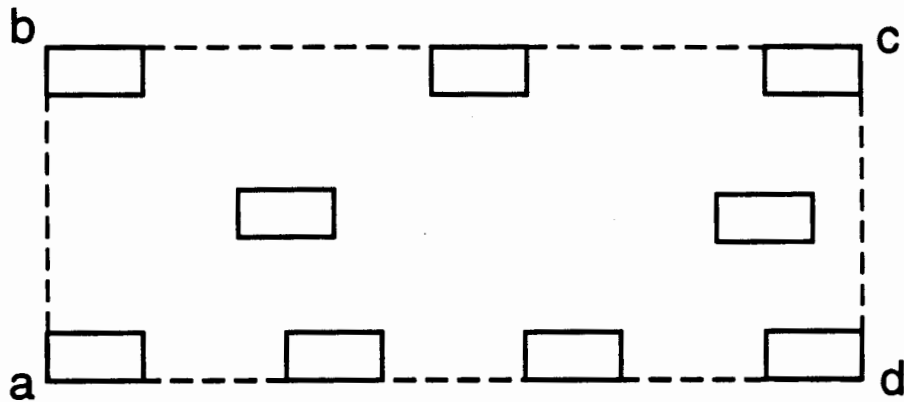


Fig. 1.

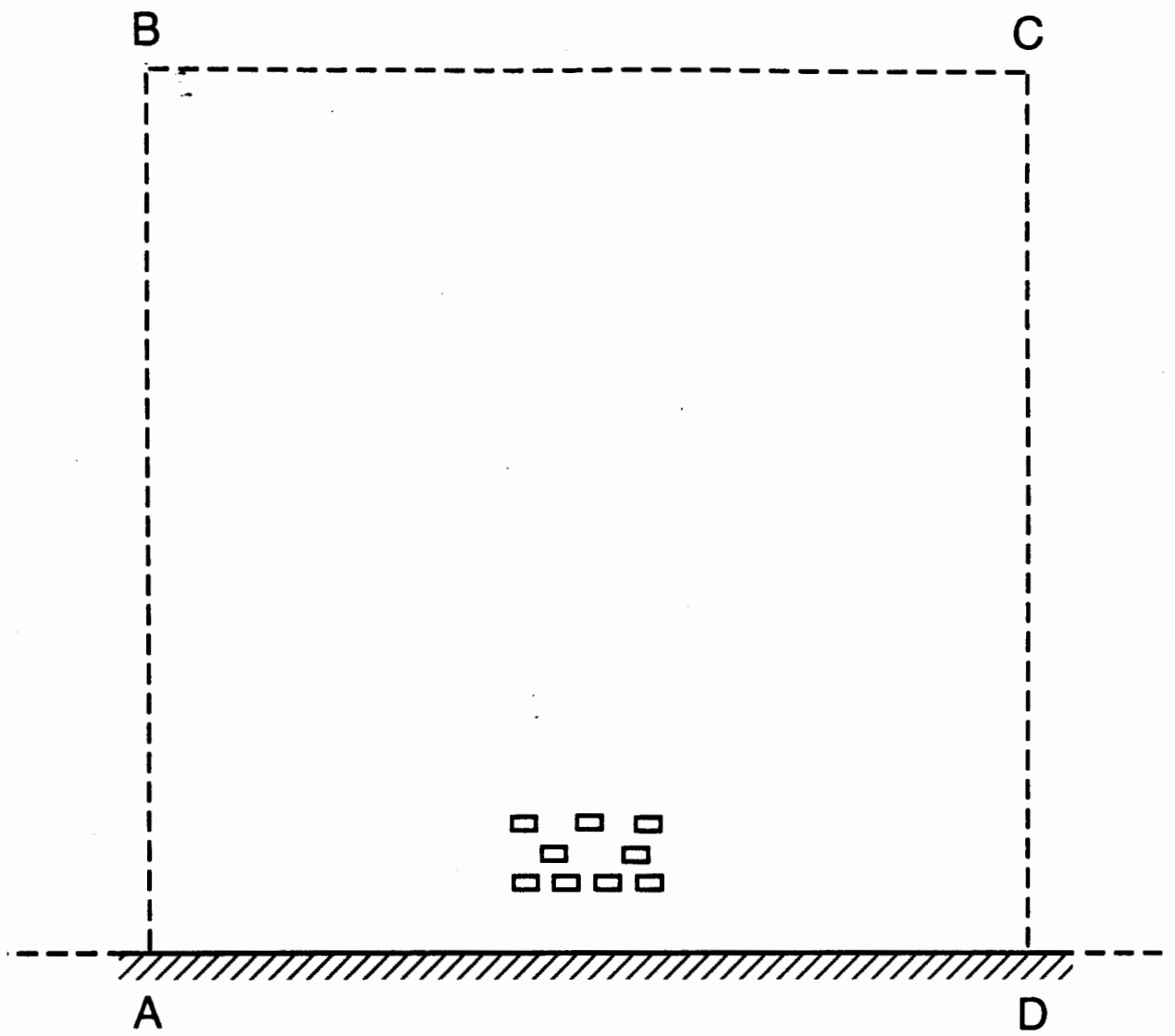


Fig. 2

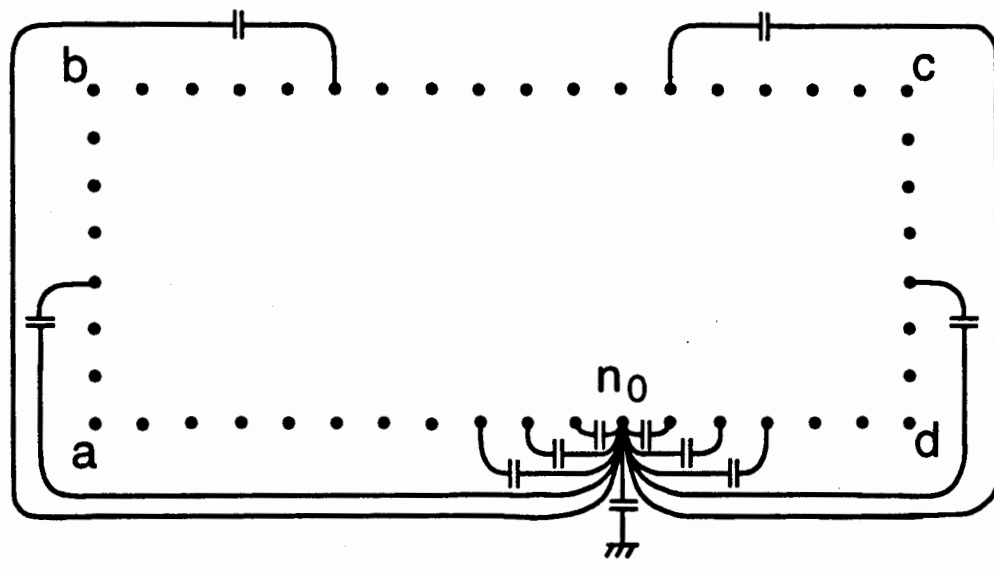


Fig. 3

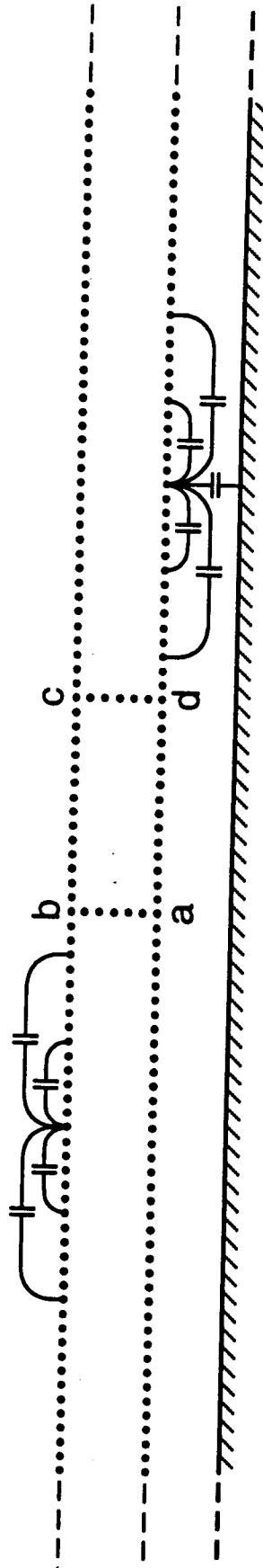


Fig. 4

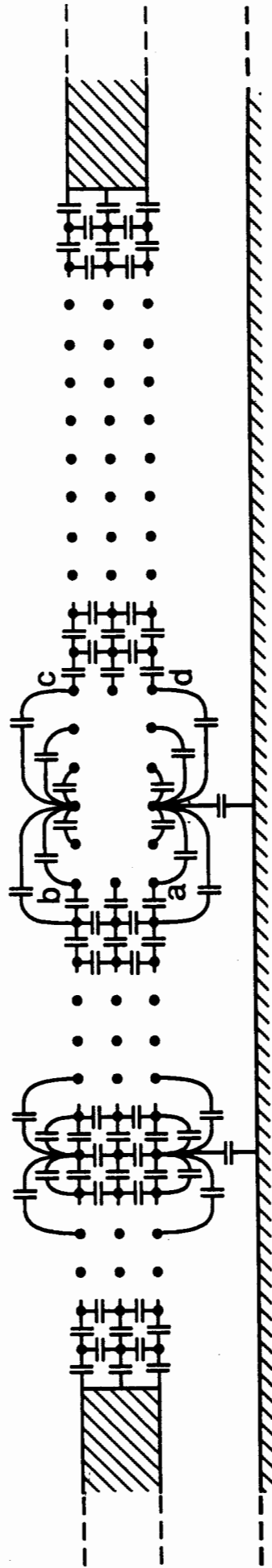


Fig. 5