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Hot Carrier Study of MOSFET at 300K and 77K

A Dissertation Presented

by

Jie Ma

to

The Graduate School

in Partial Fulfillment of the

Requirements

for the Degree of

Doctor of Philosophy

in

Electrical Engineering

Stony Brook University

December 2015

Stony Brook University

The Graduate School

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Abstract of the Dissertation

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Electrical Engineering

Stony Brook University

2015

Electronics operate at cryogenic temperature are drawing more and more attention in recent years in both aerospace area and high energy physics area. Better noise performance of cryogenic electronics than electronics at room temperature makes it a great choice for high sensitivity detectors. While typical lifetime requirement for electronics is 20 years, whether cold electronics have the required lifetime in cryogenic environment is a critical question. With regards to lifetime, the major failure mechanisms such as negative bias temperature instability (NBTI) [1], electromigration (EM), stress migration (SM), time-dependent dielectric breakdown (TDDB) and thermal cycling (TC) scale with temperature in favor of cryogenic operation [2]. The only mechanism that affects the lifetime adversely at cryogenic temperature is the degradation due to Hot-Carrier Effect (HCE). In this dissertation, HCE is studied at both 300K and 77K. The mechanism of Hot Carrier Effect is discussed and its relationship with the degradation of major device parameters including transconductance, threshold voltage, subthreshold swing and mobility is investigated. Two different measurement strategies are adopted: accelerated lifetime measurement under severe electric field stress by large V_{ds} while observing degradation in the transistor transconductance, and a separate measurement of the substrate current density as a function of $1/V_{ds}$ before and after the stress test. The former verifies the canonical very steep slope of the inverse relation between the lifetime and the substrate current density, and the latter confirms that below a certain value of V_{ds} a lifetime margin of several orders of magnitude can be achieved for the cold electronics TPC readout. The degradation of MOSFET noise due to HCE is studied at both 300K and 77K. A noise spectrum measurement system operates from 77K to 300K is designed. Measurements illustrate that PMOS exhibits a lower noise level as well as more resistant to HCE than NMOS. At both 300K and 77K, little influence of HCE on noise of PMOS can be observed makes it a good candidate as the input transistor of the pre-amplifier in the front-end ASIC which is a major noise contributor of the system. Design criteria for MOSFET based cryogenic electronics system with long lifetime and low noise degradation is proposed as a reference for circuit designers.

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Acknowledgements

I would like to thank my Ph.D. advisors, Gianluigi De Geronimo and Milutin Stanacevic for their support in the last five and half years. This work can never be delivered without their advice. I have talked with Milutin before I accepted the offer from Stony Brook University and the conversation helped me make the decision to come here. He is a very good advisor and helped me a lot. Concepts become easy to understand and interesting in his hand. I learned a lot from him. I met Gianluigi in his "Advanced Design of Low-noise, Low-power Analog Circuits" course and was attracted since then. He is a very knowledgeable and energetic man who always listen to his student. Thoughts and ideas are always respected, even the most wild ones. I am really appreciated it that he is willing to be my advisor and bring me to the Brookhaven National Laboratory (BNL). I enjoy the working atmosphere at BNL a lot. Every person is knowledgeable and willing to share their ideas. At the same place, I met my committee member Veljko Radeka. It is my honor in the life to have the opportunity to work with a worldwide distinguish scientist. His patience to students, keen insight of semiconductor and dedication to the science community impress and encourage me deeply. I would also like to give my sincerely thank to my chairman of defense, Emre Salman, for his support and valuable discussion.

I want to thank my parents for their long time support and love ever since I was born. I would like to thank all my colleges especially in the Instrumentation Division of BNL for valuable discussions and excellent technical support. I would also like to thank all my lovely friends both in China and America for the companionship in life.

Ph.D. is a long journey with excitement, frustration, joy and even self-doubt. It is the end of academic degree but not the end of learn. In the end, I would like to share with everyone the words once Veljko told me: "You will use your whole life to learn."

Chapter 1

Introduction

1.1 Background of LBNE

The Long-Baseline Neutrino Experiment (LBNE) is designed to explore the determination of the CP violation (violation of the product of the charge conjugation (C) and parity (P) symmetries), the neutrino mass hierarchy, and underground physics, including the exploration of proton decay and supernova neutrinos [3]. Figure 1.1 [4] shows the conceptual structure of LBNE. A neutrino beam travels 800 miles through the mantle to an advanced Liquid Argon Time Projection Chamber (LAr TPC) detector located at SURF, South Dakota [5]. During this journey, the oscillation asymmetry between ν and $\overline{\nu}$ due to the (non-CP-violating) matter effect will be separated from that due to true CP violation [3]. Then the high power neutrino (0.5-5 GeV) will travel through the LAr inside LAr TPC and electrons generated due to impact ionization will be collected by the sensor to reconstruct particle trajectories in 3D for analyzing [5]. 800 miles is required to be an optimal baseline for the physics goals in LBNE [6]. Since neutrinos only interact via weak force and gravity [7], no tunnel is needed [4].

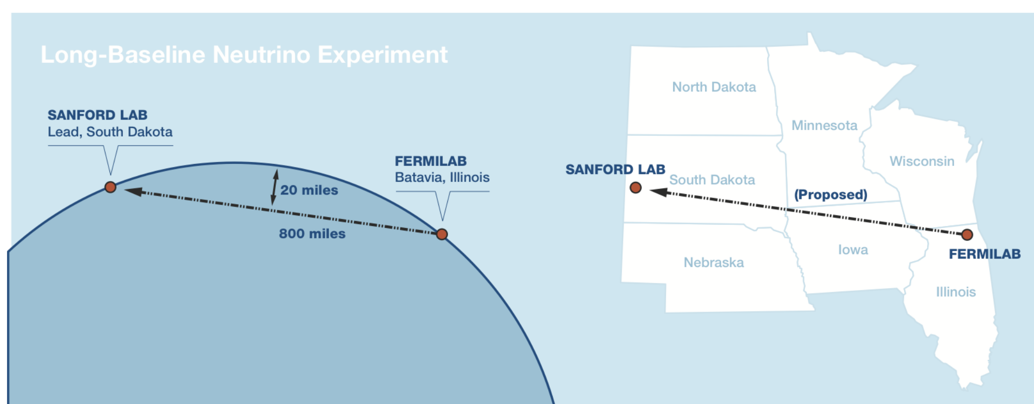


Figure 1.1: LBNE will send neutrinos through the Earth's mantle from Batavia, Illinois, to Lead, South Dakota. No tunnel is necessary for this 800 miles trip [4].

A detector element and its associated front-end electronics are illustrated in Figure 1.2. When an event happens, the sensor generates an electrical signal, which is passed to Pre-Amplifier, the Anti-Alias Filter and the Analog to Digital Converter (ADC). The digitized waveform is then used to analyze the event.

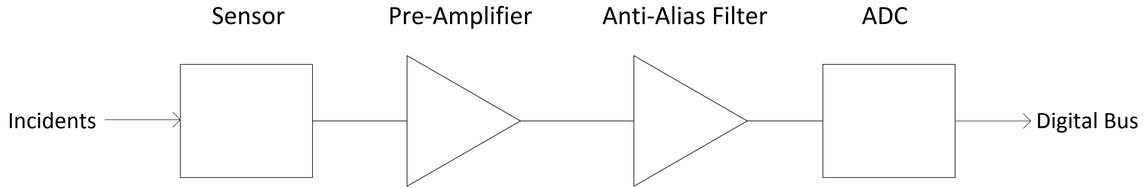


Figure 1.2: Conceptual diagram of a detector system.

The LAr TPC detector used in LBNE is made of a cryostat which contains LAr, a detector based on sensing wire immersed in the LAr, readout electronics and a cryogenic control system to keep the LAr temperature at 89 K and maintain the required purity [8]. The detector is placed at a depth of 1480 m at SURF to make the cosmic ray background contribution negligible [3].

In the cryostat, a uniform electrical field is generated between Cathode Plane Assemblies (CPA) and the Anode Plane Assemblies (APA). When the high power neutrino travels through LAr, impact ionization takes place and the generated electrons will drift towards the APA. The APA is made of three planes of sensing wires in different angles [8]. As the electrons reach the APA planes, signals will be generated on the sensing wires. The resulting waveforms are used to reconstruct the particle trajectories in 3D.

The front-end Application-Specific Integrated Circuit (ASIC) developed to operate in the LAr is described in [9]. The ASIC is located in the LAr to satisfy the requirements of low noise and extreme high purity of the LAr [8] which are described in the next section.

1.2 ASIC in LAr

1.2.1 Noise requirement

For a detection system like this, the Equivalent Noise Charge (ENC) is used to characterize the resolution of front-end electronics. The ENC is a measure of contribution to the signal from electronic noise in the front-end ASIC and corresponds to the signal charge that yields a signal-to-noise ratio of one. ENC is expressed in fC or units of electronic charges $e^- = 1.602 \times 10^{-19}C$ [10]. The front-end ASIC in LAr TPC has to be able to read up to $300fC$ ($\sim 1,873,000e^-$) and offer a resolution (which indicates ENC) less than 1000 root mean square (rms) electrons [9].

The ENC is largely depended on the total capacitance C_{total} of the sensing node, which is comprised by the sense wire capacitance, interconnect cable capacitance and gate capacitance of the input transistor in the pre-amplifier. The front-end ASIC is designed to work inside LAr and will be placed close to the end of the sensing wire. Therefore long cable is not needed and total capacitance can be greatly reduced, resulting in a better noise performance [2].

1.2.2 Purity Requirement

The LAr should be kept at a purity level of less than 200 parts per trillion (ppt) oxygen-equivalent [8] which makes outgassing of cables a critical challenge. By placing ASICs inside LAr, cables are separated into two sections: before (part 1) and after (part 2) the ASIC. The

length of cables in part 1 is negligible since ASIC is placed close to the sense wire. In part 2, the number of cables is reduced dramatically by the multiplexing circuit integrated in the ASIC. Therefore, outgassing from cables will decrease which helps to keep the high purity of LAr.

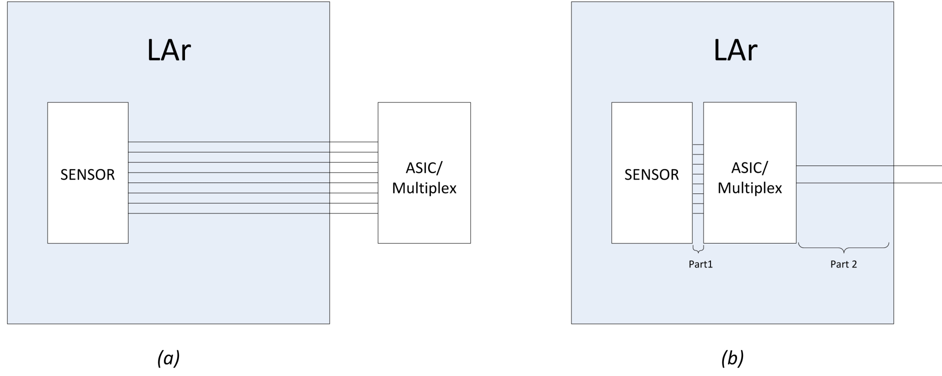


Figure 1.3: Illustration of choices (a) ASIC outside LAr, (b) ASIC inside LAr.

Additionally, by reducing the number of cables coming out of the cryostat, leakage potential at feedthrough is also reduced.

1.3 Lifetime Concern

The LAr TPC detector is supposed to operate more than 20 years during which access to electronics in the cryostat is not possible [8]. Whether cold electronics have the required lifetime in cryogenic environment is a critical question. With regards to lifetime, the major failure mechanisms such as Negative Bias Temperature Instability (NBTI) [1], electromigration (EM), stress migration (SM), time-dependent dielectric breakdown (TDDB) and thermal cycling (TC) scale with temperature in favor of cryogenic operation [2]. The only mechanism that affects the lifetime adversely at cryogenic temperature is the degradation due to Hot-Carrier Effect (HCE), which introduces trapped charges in the gate oxide of Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) as well as interface states at the $Si - SiO_2$ interface.

HCE affects many device parameters, such as transconductance, threshold voltage, mobility, drain current, subthreshold swing and low frequency noise [11–15]. Therefore it is very important to study HCE and its impact on the lifetime of MOSFET at cryogenic temperature (down to 89K). People have focused on HCE since 1980s. However most of the work is performed at Room Temperature [11,13] at linear region [11–13] while most devices in the analog front-end ASIC operate in saturation region. In this work, lifetime and parameters degradation of MOSFET due to HCE in saturation region are theoretically and experimentally investigated at both Room Temperature (300K) and Liquid Nitrogen Temperature (77K). Liquid Nitrogen is used instead of Liquid Argon to provide some temperature margin. Besides, as noise performance is very important in the front-end ASIC, the impact of HCE on low-frequency noise is also studied at both 300K and 77K.

We focus on the characteristics of NMOS devices since PMOS devices have been reported to exhibit a lifetime one or two orders of magnitude longer [16] and are not expected to be a concern in our circuit design. Measurement of PMOS devices are shown for comparison.

In this thesis, Chapter 2 presents the temperature dependency of MOSFET parameters and background of HCE including its basic mechanism and how it impacts device parameters. Study of lifetime as well as device parameters degradation including transconductance, threshold voltage, subthreshold swing and mobility during HCE are given in Chapter 3. Background of noise including basic mechanism, relationship with HCE as well as experiments designed for noise degradation measurement during HCE are discussed in Chapter 4. The conclusion is described in Chapter 5.

Chapter 2

Temperature Dependency and Hot Carrier Effect

In this chapter, background information about interface states is covered in section 1. In section 2, the temperature dependency of MOSFET's parameters (threshold voltage, mobility, subthreshold swing, drain current and transconductance) is discussed. Measurements of these parameters of the Device Under Test (DUT) ($NMOS, W = 5 \times 2\mu m, L = 180nm$) at 300K and 77K are included. The mechanism of Hot-Carrier Effect (HCE) is presented in section 3. The relationship between HCE and the degradation of threshold voltage, mobility, subthreshold swing and transconductance is discussed in the last section.

2.1 Interface States

In MOSFET, interface states are electronic energy levels located at the $Si-SiO_2$ interface that can capture or release electrons (or holes). The energy levels associated to interface states are due to the imperfections like lattice mismatch, disconnected chemical bonds or impurities [17].

According to their behavior, interface states can be categorized into donor-like interface state and acceptor-like interface state [18]. A donor-like interface state is electrically neutral when occupied by an electron and positive when the electron is released. An acceptor-like interface state is electrically negative when occupied by electron and neutral when the electron is released. Due to the ability to capture and release charge, interface states are also called interface traps. We now consider the effect of interface states for a simple case of a MOS capacitor as it is the basis to explain effects in a MOSFET. It is generally believed that at $Si - SiO_2$ interface, donor-like interface states are distributed in the lower half of the band gap while the acceptor-like interface states located in the upper half [18, 19]. As the relative position between energy level and Fermi Level (E_F) shows the occupation status of that energy level, the electrical status of an interface state is a function of band bending and gate voltage [20]. Figure 2.1 shows this dependency in a p-substrate MOS capacitor. V_{gb} is the voltage between the gate and substrate, V_{FB} is the flat band voltage and V_{mid} is the midgap voltage which indicates that the Intrinsic Fermi Level (E_i) reaches the Fermi Level at the interface of the MOS capacitor. V_{FB} can be expressed as [21]

$$V_{FB} = \phi_{MS} - \frac{Q_0}{C_{ox}} \tag{2.1}$$

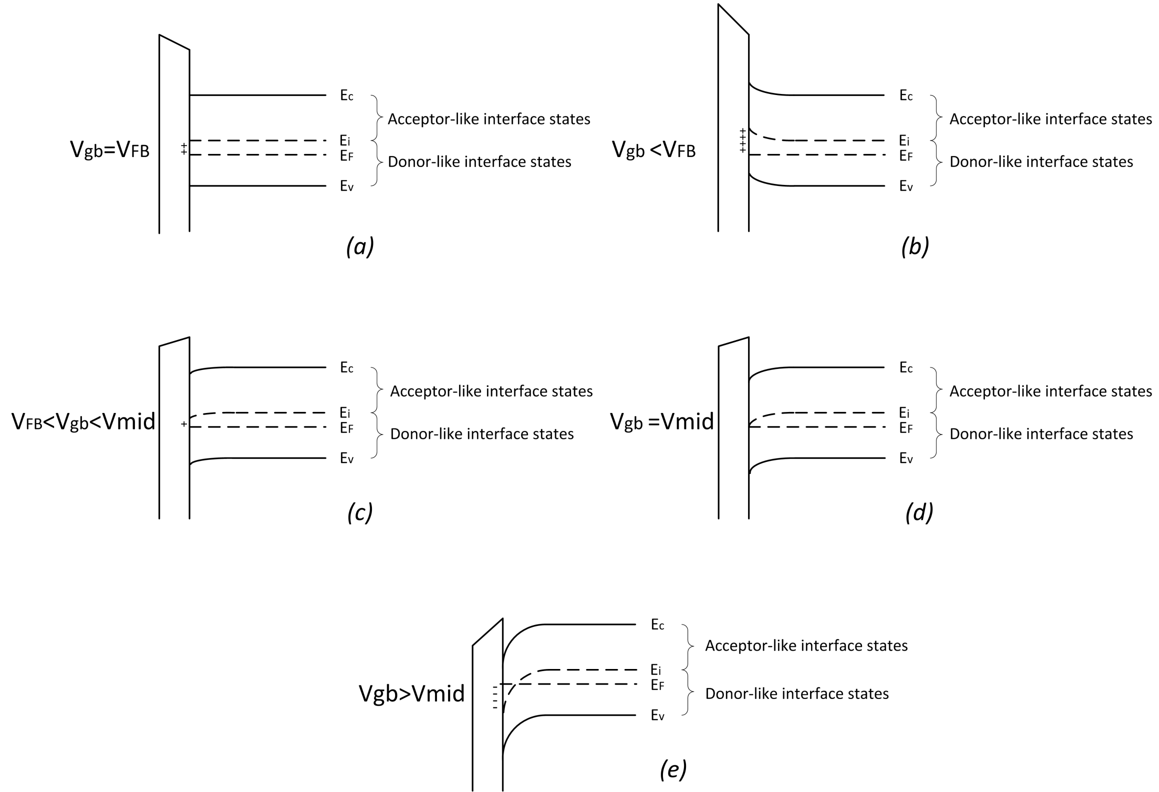


Figure 2.1: Relationship of interface state induced charges and bias voltage V_{gb} of a p-type MOS capacitor at different operating condition.(a) flatband, (b) accumulation, (c) depletion, (d) midgap, (e) inversion.

where ϕ_{MS} is the contact potential from the substrate to gate, C_{ox} is the oxide capacitance and Q_0 is the parasitic charges located at the $Si - SiO_2$ interface.

Flatband When $V_{gb} = V_{FB}$, the MOS capacitor operates in flatband condition. All acceptor-like interface states are above E_F, indicating they do not capture electrons thus are electrically neutral. Part of the donor-like interface states lie below E_F which indicates they are occupied by electrons and thus are electrically neutral while the other part of donor-like interface states lies above E_F shows electrically positive. Therefore, in the flat band condition, only donor-like interface states that are above E_F will contribute positive charges.

Accumulation When $V_{gb} < V_{FB}$, the energy band bends up. Acceptor-like interface states are still neutral while more donor-like interface states release electrons thus inducing more positive charges.

Depletion When $V_{FB} < V_{gb} < V_{mid}$, device operates in depletion region. The energy band bends down. Acceptor-like interface states are still electronically neutral while less donor-like interface states will release electrons thus less positive charges are induced.

Midgap The midgap condition is the transition point between depletion and inversion. With V_{gb} keeps increasing and E_i reaching E_F, all donor-like interface states are occupied

by electrons while all acceptor-like interface states are empty. All interface states are electrically neutral.

Inversion In inversion region, parts of acceptor-like interface states are occupied by electrons thus inducing negative charges. Other acceptor-like interface states as well as all donor-like interface states are neutral.

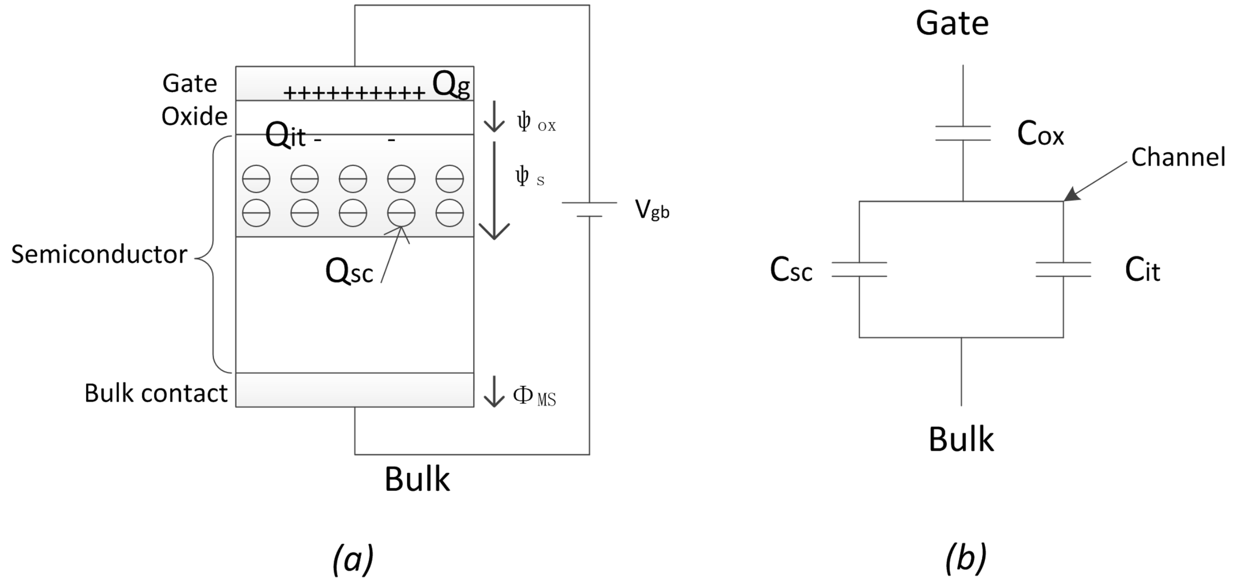


Figure 2.2: (a) Conceptual structure of a P-type MOS capacitor. (b) Equivalent circuit of MOS capacitor includes the effect of interface states [17, 21, 22].

From the above discussion, we can find that similar to a parallel-plate-capacitor in which the number of charges at the plate is controlled by the voltage between plates, charges induced by interface states are controlled by the voltage applied between the gate and bulk terminal as well. Therefore, the effect of interface states can be seen as equivalent to a capacitor. A conceptual structure of a P-type MOS capacitor including interface states in depletion region is shown in Figure 2.2 (a). In the graph, ψ_{ox} is the voltage dropping on the oxide, ψ_s is the surface potential defined as the potential drops across charge region in semiconductor, Q_g is the charge on the gate, Q_{it} is the charge induced by interface states and Q_{sc} is the charges in the semiconductor. Figure 2.2 (b) [17, 21, 22] shows the equivalent circuit model of MOS capacitor at low frequency which can be derived as the following:

The voltage drop V_{gb} can be expressed as [21]

$$V_{gb} = \psi_{ox} + \psi_s + \phi_{MS} \tag{2.2}$$

As ϕ_{MS} is the contact potential from substrate to gate thus independent of bias voltage, the change of V_{gb} can be then expressed by

$$\Delta V_{gb} = \Delta\psi_s + \Delta\psi_{ox} \tag{2.3}$$

The overall charge neutrality gives us [21]

$$Q_g + Q_{it} + Q_{sc} = 0 \tag{2.4}$$

When the external voltage changes, the charge distribution in the MOS capacitor will change as well. Following the charge neutrality, we have

$$\Delta Q_g + \Delta Q_{it} + \Delta Q_{sc} = 0 \tag{2.5}$$

For the total capacitance of the MOS capacitor at low frequency we have $C_{gb} = \frac{dQ_g}{dV_{gb}}$, thus

$$\frac{1}{C_{gb}} = \frac{dV_{gb}}{dQ_g} \tag{2.6}$$

Using Equation 2.3, we have

$$\frac{1}{C_{gb}} = \frac{d\psi_{ox}}{dQ_g} + \frac{d\psi_s}{dQ_g} = \frac{1}{\frac{dQ_g}{d\psi_{ox}}} + \frac{1}{\frac{dQ_g}{d\psi_s}} \tag{2.7}$$

Using Equation 2.5, we can obtain

$$\frac{1}{C_{gb}} = \frac{1}{\frac{dQ_g}{d\psi_{ox}}} - \frac{1}{\frac{dQ_{it}}{d\psi_s} + \frac{dQ_{sc}}{d\psi_s}} \tag{2.8}$$

Usually, $\frac{dQ_g}{d\psi_{ox}}$ is defined as the oxide capacitor and $-\frac{dQ_{sc}}{d\psi_s}$ as the semiconductor capacitor [21]. Similarly, we define $-\frac{dQ_{it}}{d\psi_s}$ as the interface state capacitor. Therefore, we can get

$$\frac{1}{C_{gb}} = \frac{1}{C_{ox}} + \frac{1}{C_{sc} + C_{it}} \tag{2.9}$$

where C_{it} is determined to be [22]

$$C_{it} = q^2 D_{it} \tag{2.10}$$

D_{it} is the interface states density.

2.2 Temperature Dependency of Parameters in MOSFET

2.2.1 Threshold Voltage

Threshold voltage is the gate bias at which strong inversion occurs which is expressed as [22]

$$V_{th} = 2\phi_F + \frac{[2qN_A\varepsilon_S(2\phi_F + \mid V_{SUB} \mid)]^{\frac{1}{2}}}{C_{ox}} + V_{FB} \tag{2.11}$$

where ϕ_F is the Fermi Potential, q is the electron charge, N_A is the doping concentration, ε_S is the permittivity of silicon, V_{SUB} is the substrate voltage and V_{FB} is the flatband voltage. ϕ_F can be expressed as [21],

$$\phi_F = \frac{kT}{q} ln \frac{N_A}{n_i} \tag{2.12}$$

where n_i is the intrinsic carrier concentration. The temperature dependency of threshold voltage mainly originates from the expression of ϕ_F. Besides the term T in Equation 2.12, n_i is also temperature dependent [22]:

$$n_i^2 \propto T^3 e^{\frac{-E_{g0}}{kT}} \tag{2.13}$$

E_{g0} is the bandgap when $T = 0K$. Therefore, by differentiating Equation 2.11, we have [22]

$$\frac{dV_{th}}{dT} = \frac{d\phi_F}{dT}(2 + \frac{1}{C_{ox}}\sqrt{\frac{\varepsilon_s q N_A}{\phi_F}}) \tag{2.14}$$

with

$$\frac{d\phi_F}{dT} \approx \frac{1}{T}(\phi_F - \frac{E_{g0}}{2q}) \tag{2.15}$$

An empirical expression of the temperature dependency of threshold voltage can also be found as [21, 23]

$$V_{th} = V_{th0} + \alpha(T - T_0) \tag{2.16}$$

where V_{th0} is the threshold voltage at temperature T_0, α is the temperature coefficient which is usually between -0.5mV/K and -3mV/K.

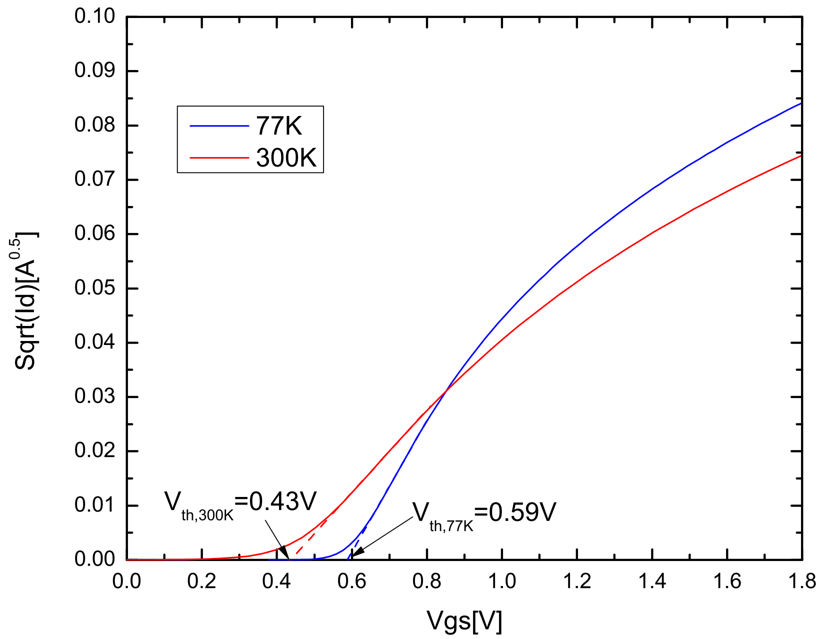


Figure 2.3: $\sqrt{Id}$ Versus Vgs at both 300K and 77K. DUT: NMOS, $W = 10\mu m(2\mu m \times 5), L = 180nm$. Tested under the condition: $V_{ds} = 1V$.

Figure 2.3 shows the threshold voltage for the NMOS device. Threshold voltage is obtained by linear fitting $\sqrt{I_{ds}}$ verse V_{gs} in the saturation region of the device. Following the expression of drain current at saturation region $\sqrt{I_{ds}} = \sqrt{\frac{1}{2}\mu C_{ox}\frac{W}{L}}(V_{gs} - V_{th})$, the ratio of the intercept to the slope of the fitting function will be $-V_{th}$. An increase of 160mV of threshold voltage from 300K to 77K is found. The temperature coefficient is then determined to be around -0.7mV/K for our technology.

2.2.2 Mobility

In semiconductor, the drift velocity (v_d) is proportional to the electric field (ε) in low electric field [21]:

$$|v_d| = \mu_B|\varepsilon| \tag{2.17}$$

The constant μ_B is the mobility. The mobility in a semiconductor is affected mainly by two scattering mechanisms: phonon scattering due to lattice vibration and coulomb scattering related to the coulomb force from ionized impurity atoms [21,22].

For MOSFET operating in inversion region, carriers flow in the inversion layer which is close to the $Si - SiO_2$ interface. In this case, additional two major scattering mechanisms exist: coulomb scattering from the interface charge and surface roughness scattering due to the surface irregularities [24]. The mobility of carriers in the inversion layer is also called surface mobility [21].

The contribution of different scattering mechanisms to the surface mobility can be combined together by the Matthiessen's rule [23,25]:

$$\frac{1}{\mu} = \frac{1}{\mu_{cb}} + \frac{1}{\mu_{int}} + \frac{1}{\mu_{ph}} + \frac{1}{\mu_{sr}} \tag{2.18}$$

where μ_{cb} and μ_{int} represent mobility limited by the coulomb scattering from the bulk ionized impurity atoms and interface charges respectively. μ_{ph} and μ_{sr} represent the mobility limited by the phonon scattering and surface roughness scattering respectively.

Temperature has different influence on each mechanism. Detailed models can be found in [29]. In general, the mobility of MOSFET is known to increase when temperature decreases following an approximation expression [21,23]:

$$\mu(T) = \mu(T_r)(\frac{T}{T_r})^{-k} \tag{2.19}$$

where T is the target temperature, T_r is the room temperature and k is a constant.

The surface mobility of the DUT is measured to be $600cm^2/Vs$ at 77K comparing to $240cm^2/Vs$ at 300K by linear fitting $\sqrt{I_{ds}}$ verse V_{gs} at the saturation region when Vds=1V.

2.2.3 Subthreshold Swing

Subthreshold swing (S) is the parameter describes how sharply the transistor can be turned off by the gate voltage (another similar concept is subthreshold slope, which is the reciprocal of subthreshold swing [22]). The definition is the gate voltage change needed to induce a drain-current change of one order of magnitude in the subthreshold area ($\frac{\Delta V_{gs}}{DecadeId}$). It can be expressed in the following equation [17,22]

$$S = (ln10)(\frac{kT}{q})(\frac{C_{ox} + C_{sc}}{C_{ox}}) \tag{2.20}$$

Temperature dependency of subthreshold swing can be mainly found in the term $\frac{kT}{q}$, which indicates a decrease of 74% ($\frac{300K-77K}{300K} \times 100\%$) in subthreshold swing from 300K to 77K.

Figure 2.4 shows the measurement of subthreshold swing. When temperature decreases from 300K to 77K, subthreshold swing decreases around 72% ($\frac{79mV/Dec(Id)-22mV/Dec(Id)}{79mV/Dec(Id)} \times 100\%$) which is very close to the theoretical value (74%).

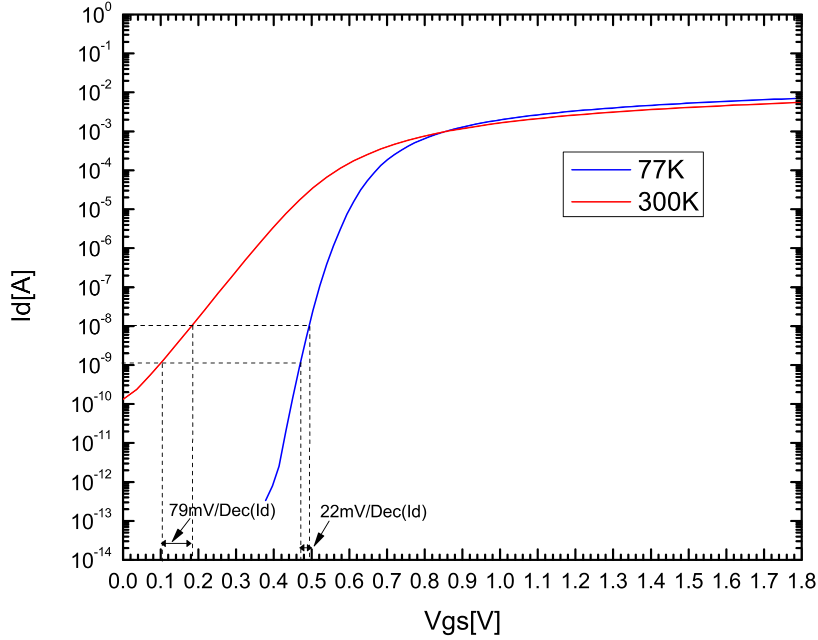


Figure 2.4: Measurement shows subthreshold swing of the dedicated technology at 300K and 77K. DUT: NMOS ($W = 10\mu m(2\mu m \times 5), L = 180nm$) under the condition: $V_{ds} = 1V$.

2.2.4 Drain Current and Transconductance

In the linear region, drain current is expressed as

$$I_d = \mu C_{ox}\frac{W}{L}[(V_{gs} - V_{th})V_{ds} - \frac{1}{2}V_{ds}^2] \tag{2.21}$$

while in the saturation region it is written as

$$I_d = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{gs} - V_{th})^2 \tag{2.22}$$

The above expression exhibits that, in both linear and saturation region, the temperature dependent components are μ and V_{th}, both of which decrease when temperature increases. They have converse effect on drain current when temperature changes.

The concept of temperature-insensitive voltage (V_{INS}) which relates to the dependency of circuit performance on temperature at different supply voltages is described in [23, 26]. The concept illustrates that a temperature-insensitive voltage exists at which the impact of temperature on drain current is minimized. Here we use the similar idea and define the temperature-insensitive voltage as the gate-source voltage in which the MOSFET has the same drain current at both 300K and 77K.

Transconductance in the linear region can be expressed as

$$g_m = \mu C_{ox}\frac{W}{L}V_{ds} \tag{2.23}$$

while in the saturation region

$$g_m = \mu C_{ox}\frac{W}{L}(V_{gs} - V_{th}) \tag{2.24}$$

In the linear region, the temperature dependency of transconductance is merely related to mobility. Therefore, when temperature increases, g_m will decrease monotonously. In the saturation region, mobility and threshold voltage affect transconductance conversely. A similar temperature-insensitive voltage as the case in drain current is expected.

Measurement of the drain current and transconductance of the NMOS DUT under the condition $V_{ds} = 1V$ at both 300K and 77K is shown in Figure 2.5. We can see when $V_{gs} = 0.87V$, the drain current reaches the same value at both 300K and 77K. This voltage is the temperature-insensitive voltage of the drain current. For transconductance, the temperature-insensitive voltage is $0.70V$.

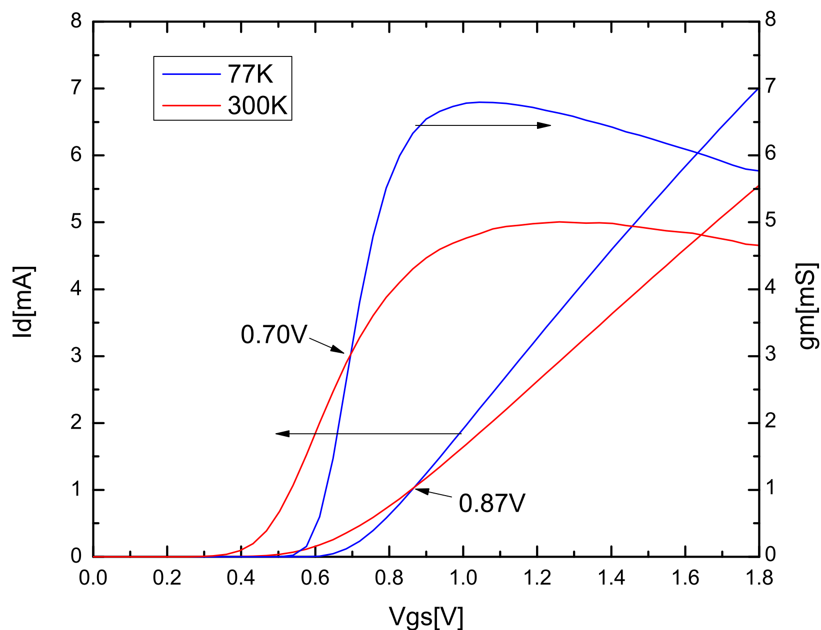


Figure 2.5: Drain current and the transconductance of the DUT at 300K and 77K. DUT: NMOS ($W = 10\mu m(2\mu m \times 5), L = 180nm$) under the condition $V_{ds} = 1V$.

Figure 2.6 shows the temperature-insensitive voltage for the drain current and transconductance at different drain voltages. By keeping gate-source voltage in the range of $0.79V \sim 0.88V$, the drain current of the transistor at 300K and 77K is largely the same while for transconductance, the region changes to $0.65 \sim 0.71V$. The temperature-insensitive voltage concept can provide circuit designers a great reference when designing circuit operating at both 300K and 77K.

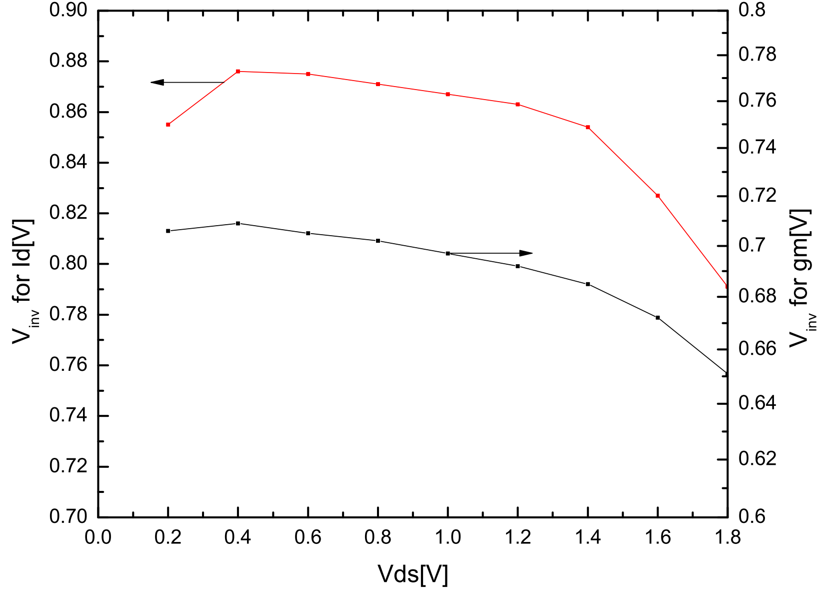


Figure 2.6: Temperature-insensitive voltage for I_d and g_m at different V_{ds}. DUT: NMOS $(W = 10\mu m(2\mu m \times 5), L = 180nm)$.

2.3 Basic Mechanism of Hot-Carrier Effects

Hot-Carrier Effects (HCE) drawn a lot of attention in the 1980s due to constant voltage scale in device which led to the rising of electric field, resulted in exacerbating HCE. The problem is released in mid-nineties when people began to reduce power supply voltage in scaling to save power as well as reduce reliability issues. However, because of non-scalability of subthreshold slope, supply voltage scaling slowed down. Therefore HCE is still a reliability issue nowadays [27]. Since the effect of hot carrier causes degradation in most cases, people also use the term hot-carrier degradation to describe this phenomenon.

In any NMOS device, electrons can become “hot” at any temperature, by attaining energy $E > kT$, where k is the Boltzmann constant, and T is the temperature. Some hot electrons exceed the energy required to create an electron-hole pair, $\varphi_i \approx 1.3eV$, resulting in impact ionization as shown in Figure 2.7. Electrons proceed to the drain. The holes drift to the substrate. The substrate current can be expressed as [11],

$$I_{sub} = C_1 I_{ds} e^{-\varphi_i / q\lambda E_m} \tag{2.25}$$

where C_1 is a constant, I_{ds} is the drain-source current, q is the electron charge, λ is the electron mean free path, and E_m is the maximum lateral electric field.

A very small fraction of hot electrons gains enough energy to be injected into SiO_2 (called hot carrier injection) as shown in Figure 2.7, during which process they can be trapped (oxide charges) or can generate interface states. Interface states are believed to dominate HCE and may result in the transistor characteristic degradation (threshold voltage, mobility, subthreshold swing and transconductance) [11]. The generation of interface states can be expressed as [11]

$$\Delta N_{it} = C_2 (t \frac{I_{ds}}{W} e^{-\varphi_{it} / q\lambda E_m})^n \tag{2.26}$$

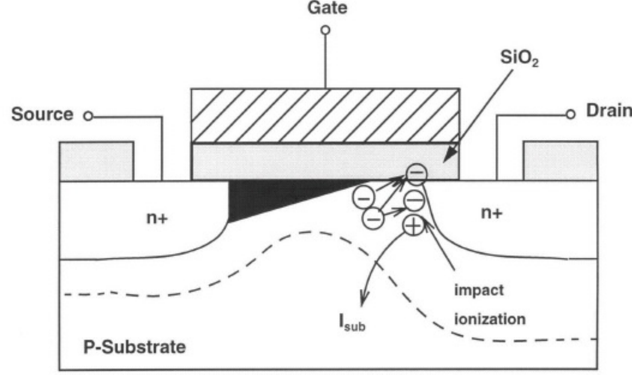


Figure 2.7: Schematic representation of impact ionization by hot electrons in the channel of an NMOS device. The holes produced by impact ionization constitute the substrate current.

where ΔN_{it} is the interface states generated during HCE, t is the time of hot carrier stress, $\frac{I_{ds}}{W}$ is the drain current density, φ_{it} is the critical energy to generate interface state and n is a constant describes how N_{it} increases with time.

The time required to change any important parameter monotonically by a specified amount, e.g. transconductance by -10%, is defined as the device lifetime [11]. The expression can be derived from Equation 2.26

$$\tau = C_3 \frac{W}{I_{ds}} e^{\varphi_{it}/q\lambda E_m} \tag{2.27}$$

where C_3 is a constant.

From the above equation, compared with 300K, a much shorter lifetime of MOSFET at 77K is expected due to the longer mean free path as phonon scattering decreases at low temperature [12].

Physical model [11] of hot electron injection can be described as hot electrons that have enough energy to surmount $Si - SiO_2$ barrier ($3.2eV$) and break the silicon-hydrogen bond ($0.3eV$) generating a trivalent silicon atom (interface state) and a hydrogen atom like

$$\equiv SiH \rightleftharpoons Si^* + H \tag{2.28}$$

If the silicon recombines with the hydrogen, no interface state will appear. If the hydrogen atom diffuses away from the interface, interface state will be generated. The total barrier for hot electrons to inject can be calculated as $\varphi_{it} = 3.2eV + 0.3eV = 3.5eV$, close to the experimental result ($\sim 3.7eV - 4.1eV$) .

It has been reported in the literature (e.g. [11, 12]) that substrate current is an efficient monitor of all hot-electron effects and it is the best predictor of a device lifetime. It is because both classes of observable hot electron effects (electrical and optical) are driven by a common driving force, the channel electric field, or more specifically the maximum channel electric field E_m located at the drain end of the channel or inside the drain terminal as shown in Figure 2.8 [28]. Therefore HCE is highly localized and happens most severely at the drain end. The substrate current I_{sub} is related to the lifetime τ (defined by any arbitrary but consistent criterion) by the relation obtained from the cancellation of $q\lambda E_m$ between 2.25 and 2.27

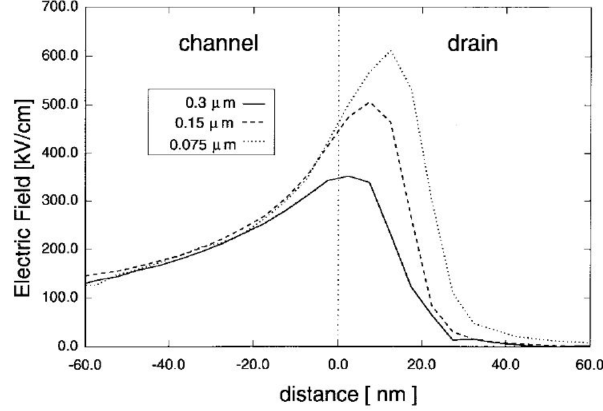


Figure 2.8: Distribution of the electric field parallel to the interface in the region close to the channel//drain boundary from Monte Carlo Simulation. Device works in the following bias condition: source $V_s = 0V$, substrate $V_b = 0V$, gate $V_g = 3V$, drain $V_d = 3V$ [28].

$$\tau = H \frac{1}{I_{ds}/W} (\frac{I_{sub}}{I_{ds}})^{-\varphi_{it}/\varphi_i} \tag{2.29}$$

where H(in $As/\mu m$) is a constant depended on the channel length, the temperature, the device technology (interface quality, drain doping, etc.), and the criterion used for the definition of lifetime. While the proportionality constant H varies from case to case, the functional relationship in 2.29 is most useful in lifetime measurements and predictions, expressed in the form,

$$\frac{\tau I_{ds}}{W} \propto \frac{1}{(I_{sub}/I_{ds})^{\alpha}} \tag{2.30}$$

where the exponent $\alpha = \varphi_{it}/\varphi_i$ is defined as the ratio of the critical electron energy to generate an interface state, $\varphi_{it}(\sim 3.7 - 4.1eV)$, and the critical energy to produce an electron-hole pair by impact ionization, $\varphi_i(\sim 1.3eV)$, in the range of about $2.9 \sim 3.2$. The ratio of these two critical energies defines the very steep dependence of the lifetime on the substrate current, and is largely independent of the temperature. Equation 2.30 is used as the main criteria for the validation of our experiments in the next chapter.

2.4 Relationship between HCE and Device Parameters Degradation

HCE affects many device parameters, such as threshold voltage, subthreshold swing, mobility, transconductance and low frequency noise. Generally speaking, HCE affects those parameters by introducing additional trapped charges inside SiO_2 and interface states. In this section, detailed information about the relationship between HCE and device parameters is discussed. Relationship between HCE and low frequency noise will be covered in chapter 4.

2.4.1 HCE and Threshold Voltage

The threshold voltage after HCE can be modeled by modifying V_{FB} as the newly generated charges play a similar role as the parasitic charges. The newly generated charges include the electrons trapped in the oxide and interface related charges (mainly charged acceptor-like interface traps), both of which are electrically negative. Therefore the flatband voltage after HCE is changed to

$$V'_{FB} = \phi_{MS} - \frac{Q_0}{C_{ox}} - \frac{(Q_{oc} + Q_{it})}{C_{ox}} \tag{2.31}$$

where Q_{oc} is the oxide charges and Q_{it} is the interface states related charges generated during HCE. The threshold voltage after HCE can be then expressed as [17]

$$V_{th} = 2\phi_F + \frac{[2qN_A\varepsilon_S(2\phi_F + \mid V_{SUB} \mid)]^{\frac{1}{2}}}{C_{ox}} + \phi_{MS} - \frac{Q_0}{C_{ox}} - \frac{Q_{oc}}{C_{ox}} - \frac{Q_{it}}{C_{ox}} \tag{2.32}$$

Therefore, the degradation of the threshold voltage due to HCE can be written as

$$\Delta V_{th} = -\frac{\Delta Q_{it}}{C_{ox}} - \frac{\Delta Q_{oc}}{C_{ox}} \tag{2.33}$$

Because oxide charges (electrons) as well as interface states (inversion region) show electrically negative, the threshold voltage will increase during HCE. As the interface states dominate HCE, Equation 2.33 can be simplified as

$$\Delta V_{th} = -\frac{\Delta Q_{it}}{C_{ox}} \tag{2.34}$$

2.4.2 HCE and Subthreshold Swing

HCE affects subthreshold swing through interface states induced charges. The trapped charges inside SiO_2 do not affect the subthreshold swing as once the degradation happens, the total trapped charges are fixed and are independent of gate bias, leading only to a horizontal shift in the curve of I_d verse V_{gs}, without changing the slope. Interface states can be modeled with as interface state capacitor in parallel with C_{sc}. Equation 2.20 can be modified as [17,22]

$$S = (ln10)(\frac{kT}{q})(\frac{C_{ox} + C_{sc} + C_{it}}{C_{ox}}) \tag{2.35}$$

Therefore

$$\Delta S \propto \Delta C_{it} \tag{2.36}$$

Subthreshold swing will increase during HCE as more interface states are generated which results in a larger interface states capacitor.

2.4.3 HCE and Mobility

Interface states induced charges degrade mobility by increasing coulomb scattering. An empirical expression [29–31] is proposed to describe the relationship between the mobility and the interface states:

$$\mu = \frac{\mu_0}{1 + \alpha N_{it}} \tag{2.37}$$

where μ is the mobility after degradation, μ_0 is the fresh mobility before degradation, α is a constant depend on the doping concentration of the substrate, N_{it} is the generated interface states during HCE. It is suggested that [29] $\alpha = -0.104 + 0.0193log(N_A)$, where N_A is the doping concentration of substrate.

Above equation can also be written as $\frac{1}{\mu} = \frac{1}{\mu_0} + \frac{\alpha N_{it}}{\mu_0}$. Therefore we have

$$\Delta\frac{1}{\mu} \propto N_{it} \tag{2.38}$$

Some researchers [31] apply a first-order Taylor Series Expansion on Equation 2.37, getting

$$\mu = \mu_0(1 - \alpha N_{it}) \tag{2.39}$$

This equation is based on the assumption that αN_{it} is always a small number [30, 31], which might not be still valid during HCE. Therefore this formula should be used with caution.

2.4.4 HCE and Transconductance

For traditional devices, the degradation of transconductance is attributed to the degradation of mobility following $\Delta g_m \propto At^n$ [32]. This power-law dependence on time no longer holds true for the Lightly Doped Drain (LDD) structure in MOSFET which is widely used now to reduce the hot carrier degradation by reducing the lateral electric field [22]. Additional degradation mechanism of increasing series resistance besides mobility results in a two stage degradation phenomena [32–34]. In the early stage of hot-carrier stress, degradation is primarily due to the accumulation of negative charges underneath the LDD spacer which increases the parasitic drain series resistance by creating a depletion region as shown in Figure 2.9. The increasing of series resistance eventually saturates as enough negative charges has been trapped to induce surface inversion which limits the further increasing of depletion width. After that, the degradation of transconductance will enter the later stage when the degradation is primarily due to the mobility reduction from interface states induced charges outside of the LDD region. The mobility reduction exists throughout both of the two degradation stages [32]. A method to extract the contribution to transconductance degradation from mobility and series resistance is proposed in [35].

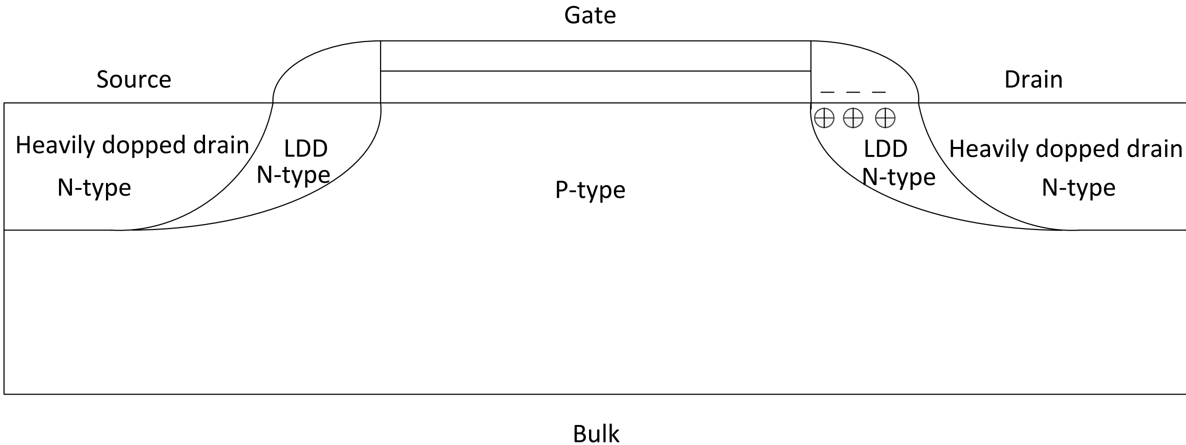


Figure 2.9: Early stage of hot-carrier degradation in NMOS with LDD structure.

Chapter 3

Lifetime Prediction and Device Parameters Degradation

In this chapter, the concept of Accelerated Lifetime Test (ALT) is firstly discussed. Then a new constant current stress and measurement strategy is proposed and adopted in our ALT at both 300K and 77K. Measurements are verified. Lifetime prediction and device parameters degradation during HCE are then discussed.

3.1 Accelerated Lifetime Test

The lifetime of a transistor is supposed to be many years. Therefore for lifetime study, ALT is required to bring the lifetime tests to a practical duration and the actual lifetime is extrapolated from that. The basic idea of ALT is to place the device in the environment that exceeds the normal operating condition in order to accelerate the degradation process and use the data to extrapolate the actual lifetime of the device in the desired operation condition. Here, we stress the device in a severe lateral electric field by providing a much higher drain-source voltage (Vds_{stress}) than the nominal core voltage (1.8V for our technology). A group of ALT is performed for each size of transistor at each operation temperature to gain enough information for lifetime prediction. For example, for devices with minimal length, Vds_{stress} is selected to be 2.8 V, 3.0 V, 3.1 V and 3.2 V at 300K and 2.8 V, 3.0 V and 3.2 V at 77K.

NMOS is used for the lifetime studies since PMOS device exhibits a lifetime one or two orders of magnitude longer than that of a NMOS device [16] and it is not expected to be a concern in our circuits. The DUT is fabricated in a commercial CMOS $0.18\mu m$ technology from Taiwan Semiconductor Manufacturing Company (TSMC). The channel lengths L adopted in our measurements are 180nm and 270nm and the channel width is $10\mu m$ in 5 fingers with $2\mu m$ each. The layout of device with $L = 180nm$ is shown in Figure 3.1 [36]. The minimal length device is the primary study object because it represents the worst-case degradation compared to longer channel devices at given stress condition. This is because a shorter length results in a higher electric field, thus a higher proportion of hot carriers will be generated leading to a more severe hot carrier effect [12]. Devices with the length of 270nm are studied for comparison. The stress condition for the longer devices are $Vds_{stress} = 3.2V, 3.3V, 3.4V$ at 300K and $Vds_{stress} = 3.1V, 3.2V, 3.3V$ at 77K. The DUTs are designed to have negligible voltage drop across any parasitic resistance and to dissipate a power less than 15mW in stress

tests to prevent temperature change due to self-heating [36].

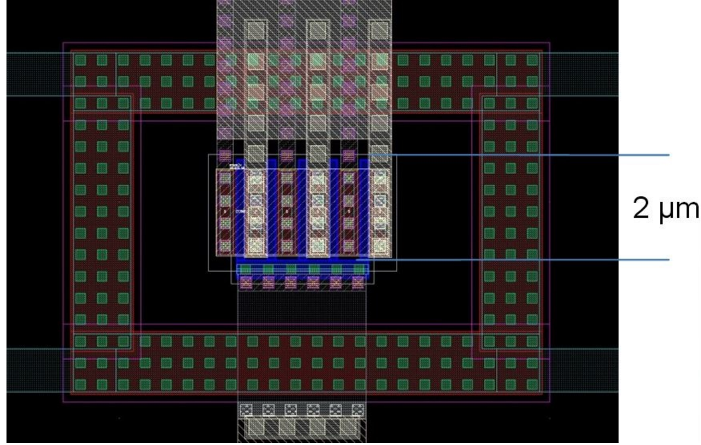


Figure 3.1: Layout of the NMOS DUT (180nm case), $W = 10\mu m(5fingers \times 2\mu m)$ [36].

In the stress test, we follow the criterion for lifetime typically adopted in the literature [12] : 10% degradation of transconductance. The stress test is composed of two steps: accelerated stress (stress) and parameter measurement (test). Parameter measurement is performed first and accelerated stress follows. Then parameter measurement is performed again and judgment of whether the criterion is met (10% degradation in transconductance) is made. The experiment is finished if transconductance has degraded for 10%, otherwise another accelerated stress is performed and followed by another parameter measurement. The drain current in stress steps and parameter measurement steps are both predefined and kept the same during each stress and measurement. The drain current in accelerated stress and parameter measurement step is set to be the drain current of fresh device under the condition that $V_{ds} = Vds_{stress}, V_{gs} = 1V$ and $Vds_{test} = V_{gs} = 1V$ respectively. The procedure can be summarized in the following steps ($Vds_{stress} = 2.8V$ as an example).

1. Initial transconductance ($gm_{initial}$) and test current(Id_{test}) are measured at the condition $Vds_{test} = Vgs_{test} = 1V$ with source and bulk connected to the ground. We also measure the stress current (Id_{stress}) at the condition $V_{ds} = Vds_{stress}, V_{gs} = 1V$. Vds_{stress} is 2.8V in this example. The gate voltage for stressing Vgs_{stress} is set to 1V initially.

2. DUT is stressed at the condition $V_{ds} = Vds_{stress}, V_{gs} = Vgs_{stress}$ for T second.

3. Transconductance(gm) is measured at the condition $Vds_{test} = 1V, I_{ds} = Id_{test}$. We do not measure the transconductance at the condition of $Vds_{test} = Vgs_{test} = 1V$ as before because during accelerated stress step, HCE decreases the mobility and increases the threshold voltage. To keep the test current a constant, we have to increase the gate-source voltage. For similar reason, we have to measure the gate-source voltage Vgs_{stress} at the condition $V_{ds} = Vds_{stress}, I_{ds} = Id_{stress}$ again to keep the stress current constant.

4. Degradation of transconductance is calculated following $\Delta gm = \frac{gm_{initial} - gm}{gm_{initial}} \times 100\%$

5. If $\Delta gm \geq 10\%$, ALT is finished. Otherwise steps $2 - 5$ are repeated.

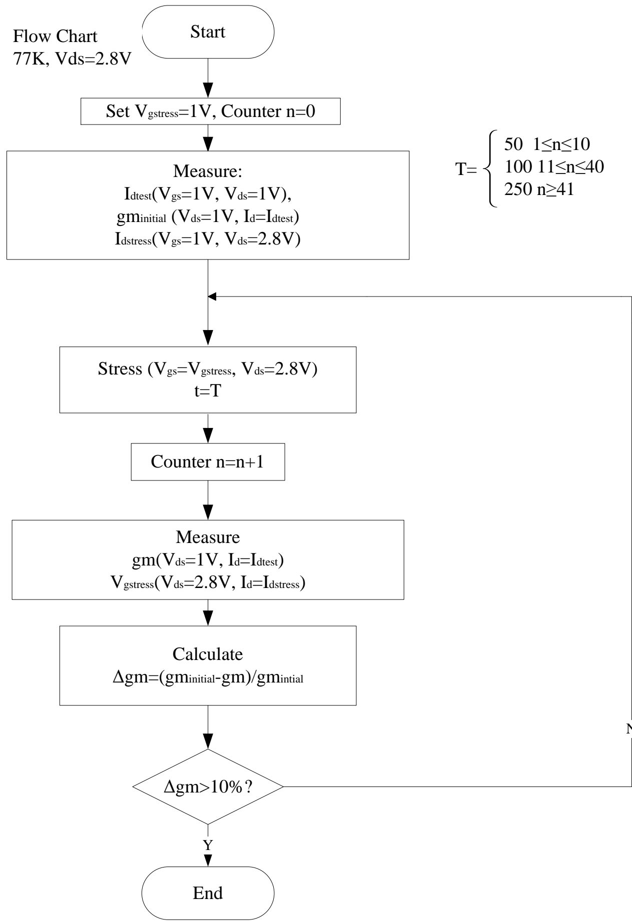
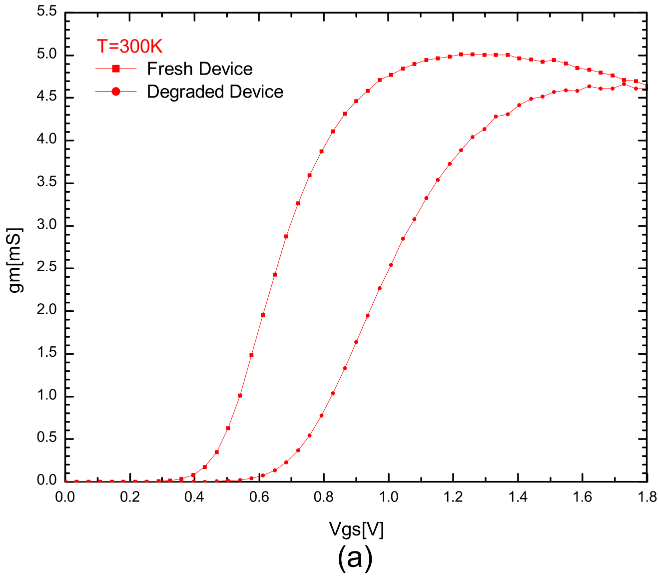


Figure 3.2: Flow chart of ALT.

To better illustrate the procedure, a flow chart of the test experiment is shown in Figure 3.2.

Figure 3.3 shows the change of transconductance before and after hot carrier stress at both 300K and 77K. As we evaluate transconductance under constant current strategy, transconductance is re-plotted verse drain current as shown figure 3.4.

Hot carrier stress, when interface states are generated, is performed in the accelerate stress step. The parameters used to study degradation are measured during the parameter measurement step. In the parameter measurement step, different Δgm is found at different operating condition even after the same amount of stress. To investigate the impact of operating condition of the DUT in parameter measurement step on degradation data, we designed an additional experiment. The stress step is the same as stated before while the parameter measurement step is changed to the following: transconductance is measured at multiple drain-source voltages (0.1V, 0.5V, 1V and 1.8V respectively) after each stress step. Figure 3.5 shows the degradation of transconductance. The device is stressed with $Vds_{stress} = 3.2V$ at 300K. The stress time represents the amount of the stress. From Figure 3.5 we can see that at a certain stress time, 10000s for example, the transconductance degradation can vary from 8% to 30% at different device operating conditions in measurement step (different Vds_{test}). Lifetime result



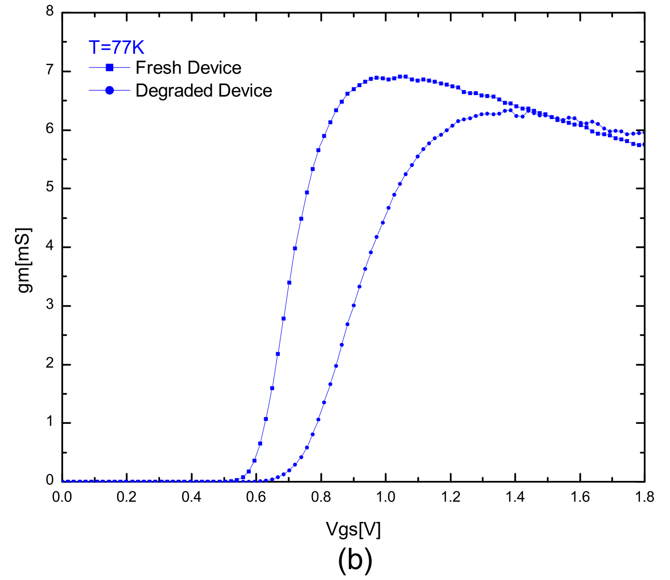
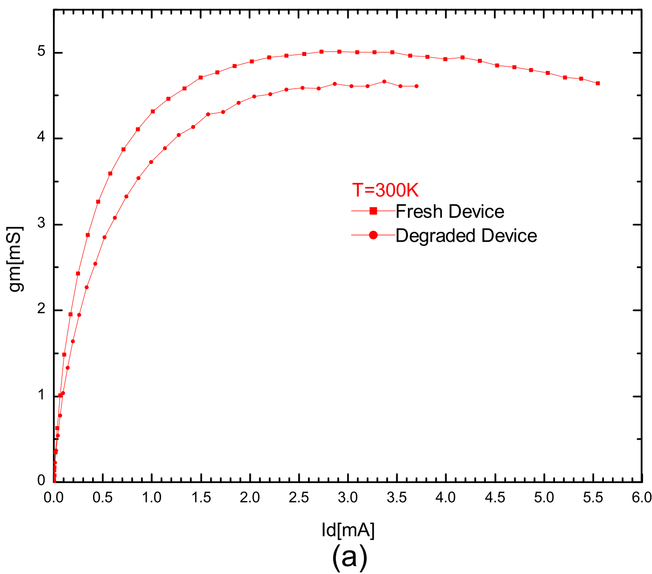


Figure 3.3: Transconductance verse Vgs of the fresh and degraded device at (a)300K and (b)77K



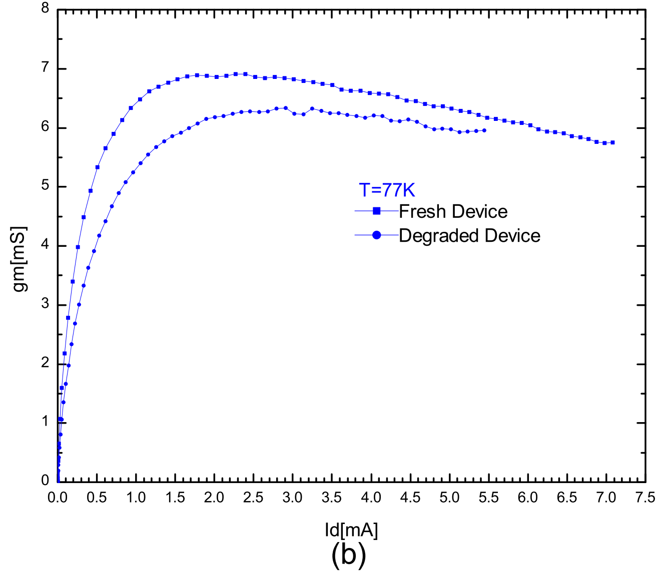


Figure 3.4: Transconductance verse Id of the fresh and degraded device at (a)300K and (b)77K

(10% degradation in transconductance) is therefore highly depended on Vds_{test}. Up to two orders of magnitude difference in lifetime can be observed (300s when $Vds_{test} = 100mV$ and 30000s when $Vds_{test} = 1.8V$). The less severe degradation of transconductance in the latter case can be explained as the following: increasing Vds releases the energy band bending at the drain side where most of the hot carrier injection induced interface states locates; therefore, as described in Chapter 2, more acceptor-like interface states will be discharged, resulting in less impact of interface states on device parameters. Thus a reasonable operating condition at parameter measurement step is essential for lifetime evaluation according to the application.

We adopt $Vds_{test} = 1V$ as it is a more realistic operation condition in analog circuit (DUT operates in the saturation region) rather than the traditionally operation condition(Vds=0.1V, i.e. DUT operates in the linear region) [11, 31, 37] for hot carrier studies.

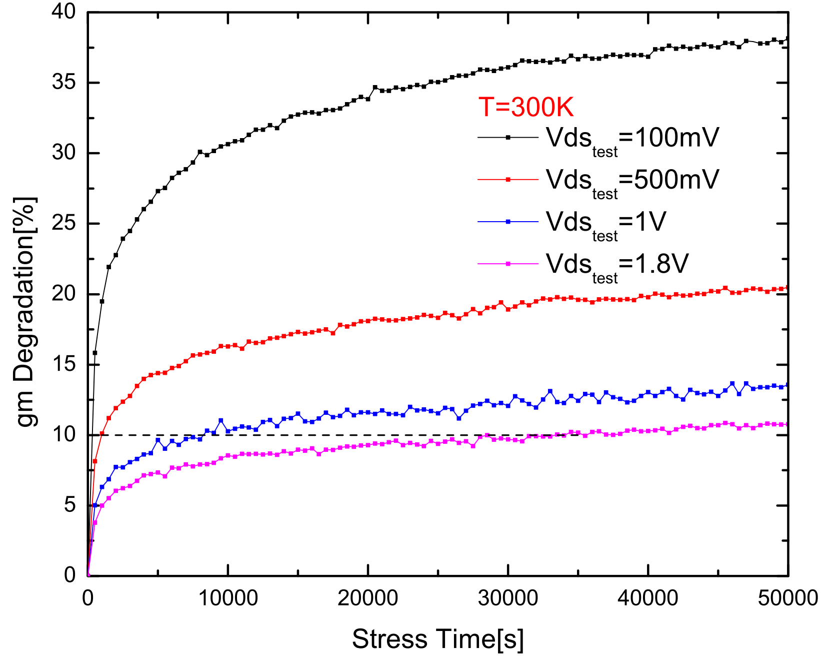


Figure 3.5: Transconductance degradation measured at different operating conditions under the same amount of stress.

3.2 Validation of Test Result

The degradation results of transconductance versus stress time for NMOS devices are shown in Figure 3.6. The ALT parameters are summarized in table 3.1. Using those data, we can verify our experiment following Equation 2.30 :

$$\frac{\tau I_{ds}}{W} \propto \frac{1}{(I_{sub}/I_{ds})^{\alpha}} \tag{3.1}$$

If we plot $\frac{\tau I_{ds}}{W}$ versus $\frac{1}{I_{sub}/I_{ds}}$ in logarithmic scale, devices with the same size and stressed at the same temperature should fall in a line with a slope of $-\alpha$ which should be in the range between -2.9 and -3.2.

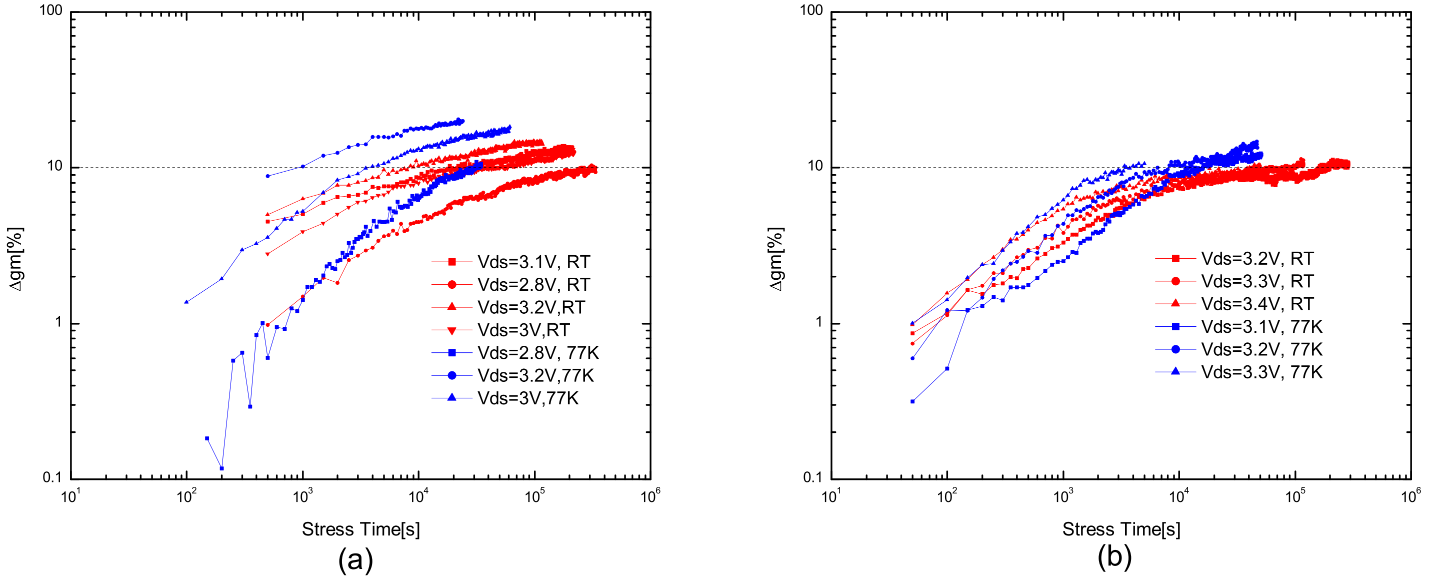


Figure 3.6: Transconductance degradation of NMOS transistors at 300K and 77K with the size of $W = 10\mu m(5 \times 2\mu m), L = (a)180nm, (b)270nm$.

Table 3.1: List of stress voltage (Vds_{stress}), substrate current during stress(Ib_{stress}), drain current during stress (Ids_{stress}), lifetime (τ) of NMOS transistor ($W = 10\mu m(5 \times 2\mu m)$) at 300K and 77K.

Length[nm]	$T[K]$	$Vds_{stress}[V]$	$Ib_{stress}[A]$	$Id_{stress}[A]$	$\tau[s]$
180	300	2.8	5.50×10^{-5}	2.09×10^{-3}	331069
		3.0	1.03×10^{-4}	2.25×10^{-3}	42796
		3.1	1.42×10^{-4}	2.22×10^{-3}	222852
		3.2	1.87×10^{-4}	2.36×10^{-3}	8506
	77	2.8	7.24×10^{-5}	3.35×10^{-3}	30717
		3.0	1.47×10^{-4}	4.01×10^{-3}	3564
		3.2	2.88×10^{-4}	4.51×10^{-3}	928
270	300	3.2	7.72×10^{-5}	1.30×10^{-3}	188975
		3.3	9.84×10^{-5}	1.38×10^{-3}	95591
		3.4	1.34×10^{-4}	1.44×10^{-3}	46318
	77	3.1	8.74×10^{-5}	1.93×10^{-3}	15783
		3.2	1.19×10^{-4}	1.90×10^{-3}	7697
		3.3	1.57×10^{-4}	2.10×10^{-3}	3604

Figure 3.7 shows the validation result. The slopes of fitting lines fall well in the theoretical region. Only devices with the length of 270nm stressed at 77K slightly falls off by 3%.

The PMOS device ($W = 10\mu m(5 fingers \times 2\mu m), L = L_{min} = 180nm$) has also been tested for comparison using the same constant current strategy. The degradation of the transconductance of the PMOS is shown in Figure 3.8. Compared with Figure 3.6, the degradation in the PMOS is much slower than NMOS. For a comparable stress time when NMOS reaches 10% degradation in transconductance, PMOS only experience less than 2% degrada-

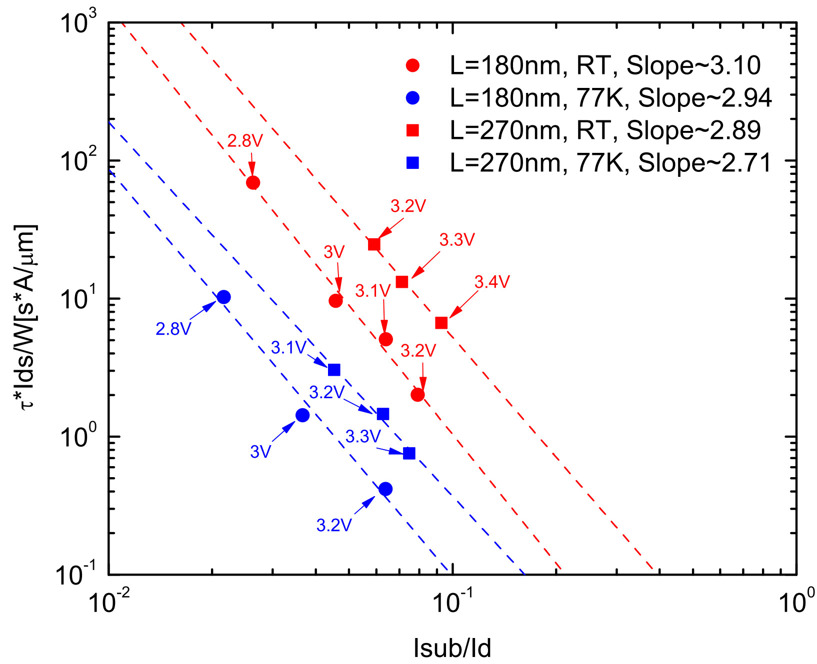


Figure 3.7: Validation of measurement at both 300K and 77K.

tion. Therefore, the lifetime of NMOS will be the critical one of our front-end ASIC and it will be discussed in the next section.

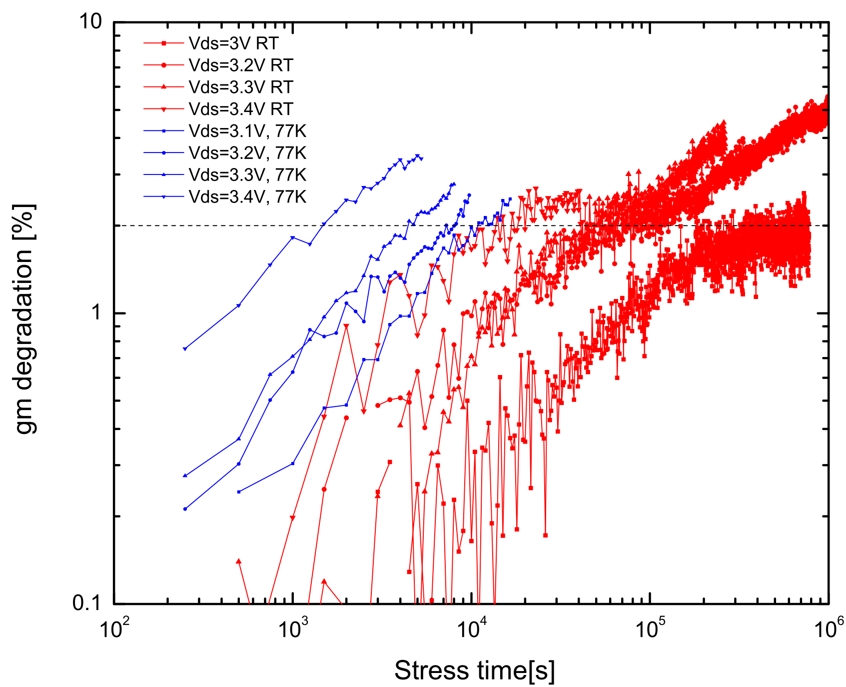


Figure 3.8: The degradation of transconductance of PMOS device.

3.3 Lifetime Projection

The lifetime projection is based on the empirical equation [12, 38]:

$$\tau \propto e^{\frac{C}{V_{ds}}} \tag{3.2}$$

where C is a constant which depends on technology. By taking logarithm of both sides of the equation we have

$$log_{10}\tau \propto \frac{1}{V_{ds}} \tag{3.3}$$

If we plot the lifetime over the reciprocal of the drain-source voltage in the semi-log curve, the data points from DUTs with the same operation temperature and channel length should fall into a straight line. By extrapolating the fitting line we can have a reasonable estimate of the device lifetime operated at the target Vds. This approach is widely adopted in lifetime predictions [12, 16, 38, 39].

The lifetime is extrapolated when Vds equals the core voltage (1.8V). From Figure 3.9 we can see the lifetime of NMOS of the minimal length can be extrapolated as 5.9×10^3 years at 77K and 1.0×10^5 years at 300K. The lifetime of the device at 77K is about one order of magnitude shorter than that at 300K. The difference can be explained as phonon scattering decreases at low temperature, resulting a longer mean free path, thus a higher proportion of hot carriers which leads more severe HCE [12]. However it is important to observer that by reducing maximum drain-source voltage at 77K by 7% (i.e. from 1.8V to 1.67V) makes the lifetime equal to that at 300K.

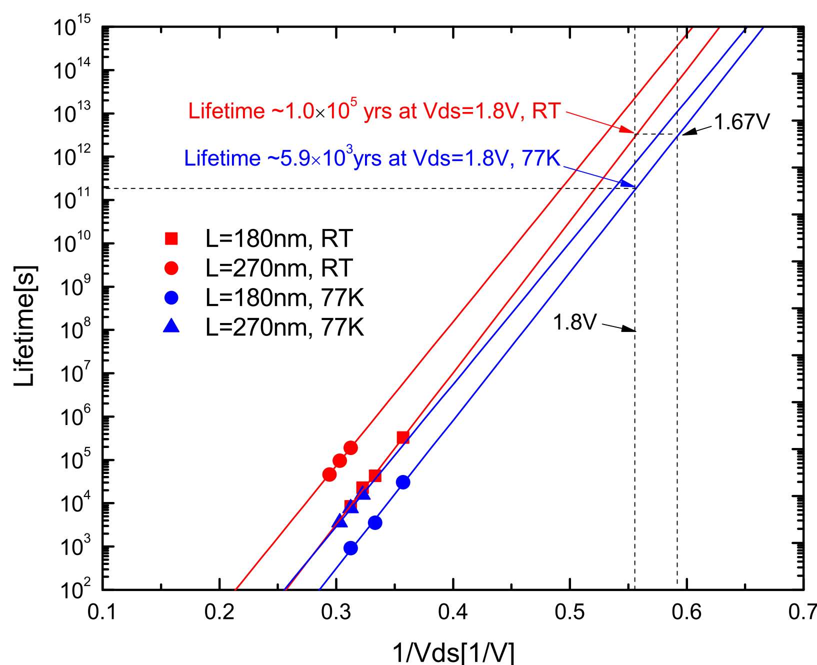


Figure 3.9: Lifetime projection using data shown in table 3.1.

Figure 3.10 shows that device with a longer length has a longer lifetime. Stressed with drain-source voltage 3.2V at 77K, device with the length of 270nm has nearly one order of

magnitude longer lifetime than the device with the length of 180nm as shown in Figure 3.9. The reason has been illustrated earlier in this chapter: the shorter length device has a much higher electric field under the same operating condition, thus a higher proportion of hot carriers will be generated leading to a more severe hot carrier effect [12].

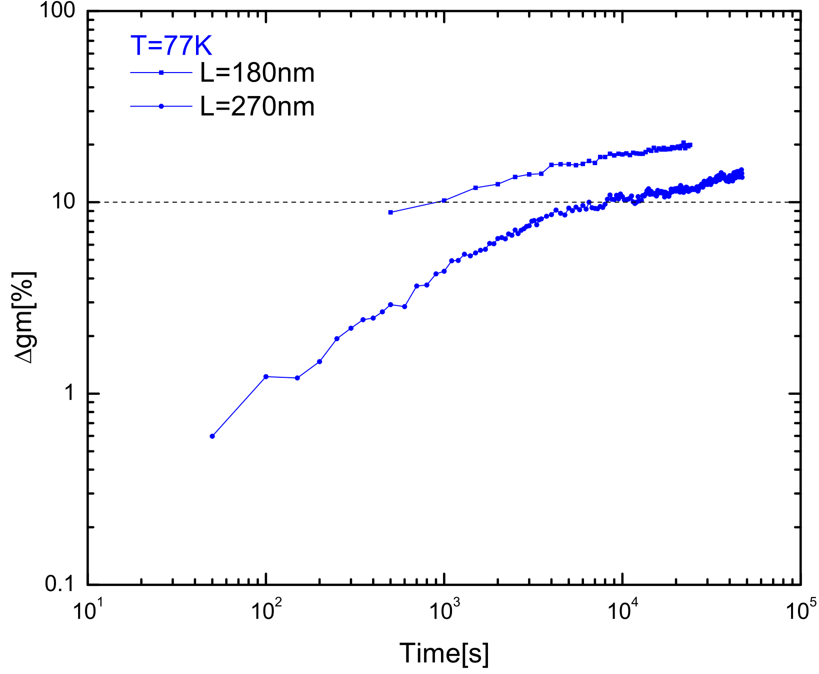


Figure 3.10: Lifetime of devices with different lengths. Device stressed at the condition of: Vds=3.2V at 77K.

We propose another way to project the lifetime. It is based on the observed result that lifetime is proportional to the reciprocal of the third order of substrate current density [11,20]. Considering $\varphi_{it}/\varphi_i \sim 3$, this relationship can also be derived from Equation 2.29

$$\tau = H\frac{1}{I_{ds}/W}(\frac{I_{sub}}{I_{ds}})^{-\varphi_{it}/\varphi_i} \approx H\frac{(\frac{I_{ds}}{W})^2}{(\frac{I_{sub}}{W})^3} \tag{3.4}$$

The drain current density from the highest stress condition (3.2V) to the target operation condition (1.8V) changes 47% at 77K and 24% at 300K while substrate current density changes more than two orders of magnitude at both 77K and 300K. Therefore, in the interested region for lifetime prediction (drain source voltage from 3.2V to 1.8V), comparing to substrate current density, the drain current density keeps largely the same and can be traded as part of the coefficient. Equation 3.4 can be then written as

$$\tau \propto (\frac{I_{sub}}{W})^{-3} \tag{3.5}$$

Thus, lifetime in the target operating condition can be predicted using the following equation:

$$\tau_{target} = (\frac{I_{sub,stress}/W}{I_{sub,target}/W})^3 \tau_{stress} \tag{3.6}$$

where τ_{target} and τ_{stress} represent lifetime at the target operating condition and stress condition respectively while $I_{sub,target}$ and $I_{sub,stress}$ represent the substrate current at target condition and stress condition respectively. Figure 3.11 illustrates that the lifetime of NMOS of the minimal length at 77K is 4300 years while at 300K is 8300 years using this method.

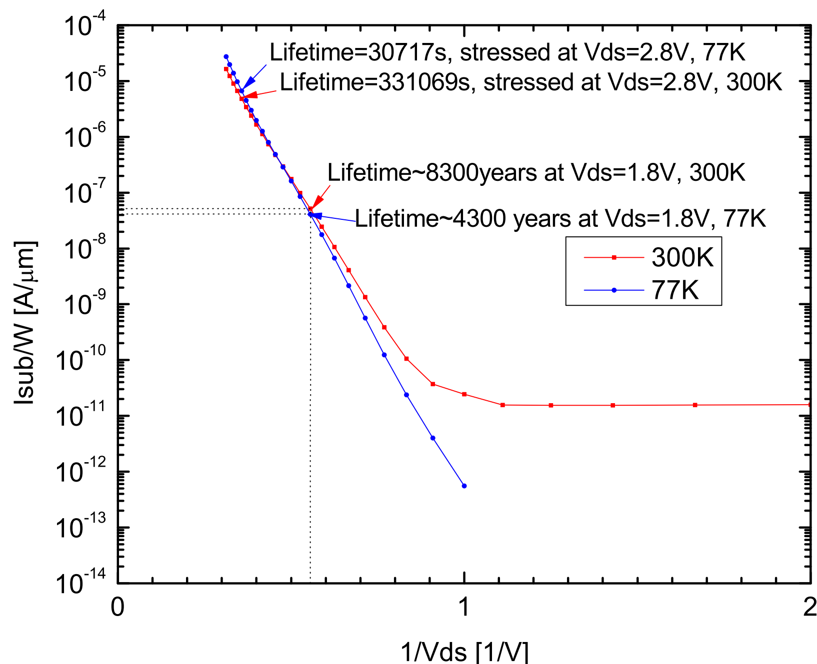


Figure 3.11: Substrate current density verse $1/V_{ds}$ for NMOS transistor of $L = 180nm, W = 10\mu m(5 \times 2\mu m)$ at both 77K and 300K. Vgs=1V. The core voltage is 1.8V for the device. ALT is performed when V_{ds}=2.8V at 77K and 300K. $V_{ds} = 1.8V$ is selected as the target operation condition for lifetime extrapolation.

This method offers a convenient alternative way to estimate the lifetime of a process. For a given condition (technology, size of device, temperature, etc), all information needed is the substrate current density at different V_{ds} plus only a single ALT. This method is less accurate due to the device variation since only one device is used and substrate current density may vary for different devices. But as the predicted lifetimes are about two orders of magnitude longer than the time of interest for the physics experiments (20-30 years), such an uncertainty in the predicted very long lifetimes is not a concern for practical use.

In the low-power analog front-end ASIC for LAr TPC [9], all transistors are well below the nominal core voltage of 1.8V with length longer than the minimal value 180nm. The distribution of I_{sub}/W and $1/V_{ds}$ of all NMOS analog transistors in the ASIC is shown in Figure 3.12 [36]. The effect of hot carrier injection on lifetime of the ASIC is thus negligible in the interested range of operation (up to 30 years) even at 77K.

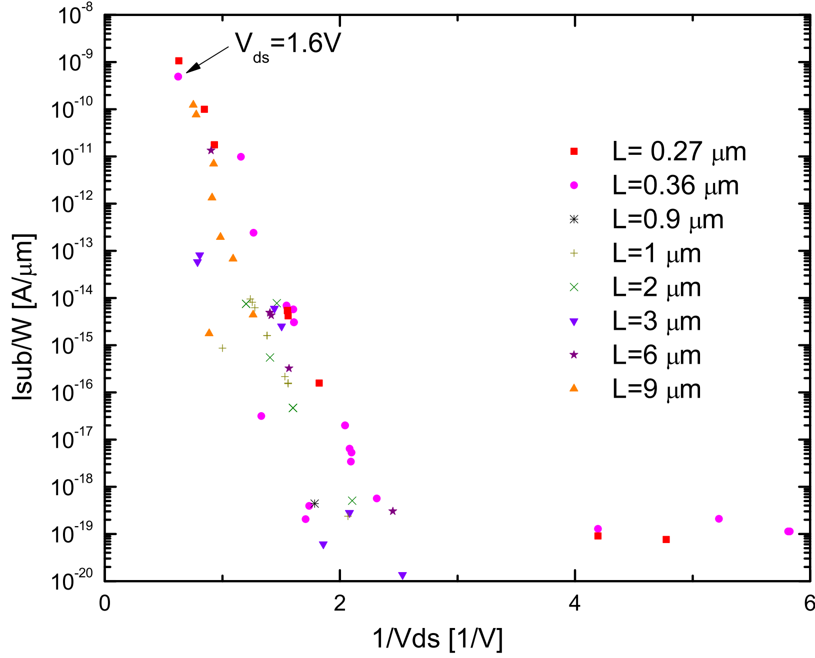


Figure 3.12: I_{sub}/W and $1/V_{ds}$ distribution for all NMOS transistors in the analog front-end ASIC for LAr TPC [9]. $V_{ds} < 1.6V$ results in a small hot carrier degradation and very long extrapolated life time.

3.4 Degradation of Device Parameters

The degradation of transconductance is already covered in the previous sections. In this section, the degradation of the threshold voltage, subthreshold swing and mobility during hot carrier stress are presented.

3.4.1 Threshold Voltage

Figure 3.13 shows how the threshold voltage changes after hot carrier stress at both 300K and 77K.

The threshold voltage is obtained by linear fitting $\sqrt{I_{ds}}$ verse V_{gs} in the saturation region of the device. Following the expression of drain current at saturation region $\sqrt{I_{ds}} = \sqrt{\frac{1}{2}\mu C_{ox}\frac{W}{L}}(V_{gs} - V_{th})$, the ratio of the intercept to the slope of the fitting function will be $-V_{th}$. The threshold voltage is extracted after each stress step. Results are shown in Figure 3.14. The threshold voltage increases during HCE as expected.

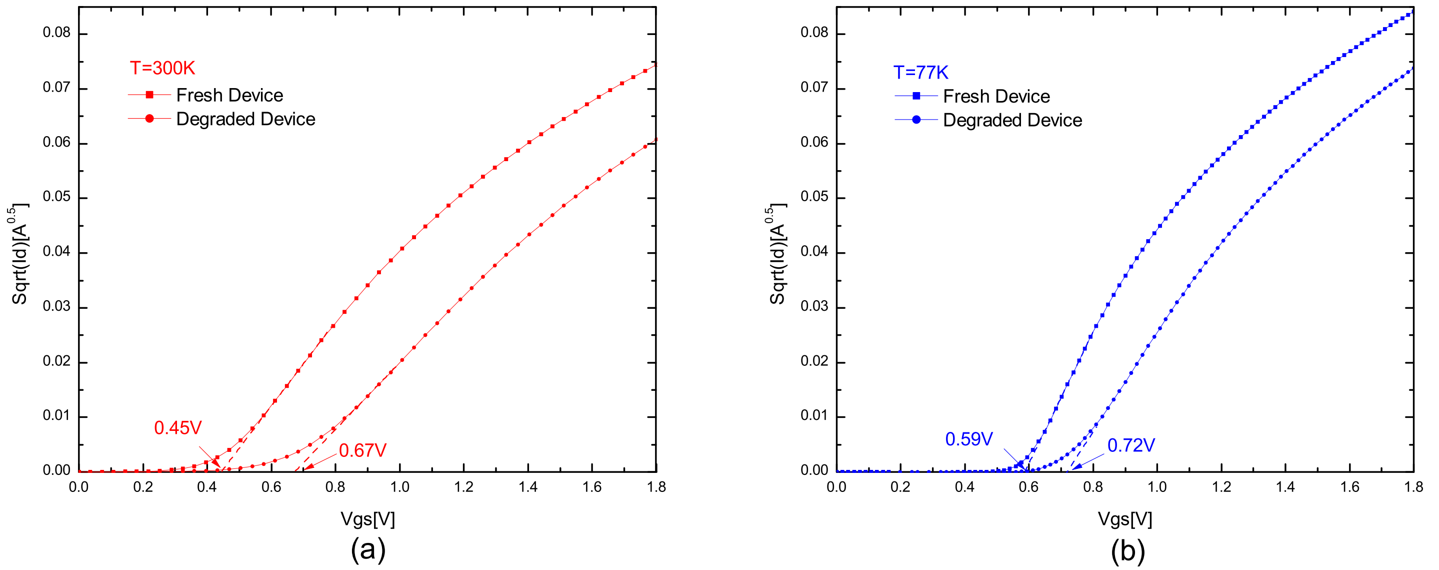


Figure 3.13: Threshold voltage of the fresh and degraded NMOS device with minimal length at (a)300K and (b)77K

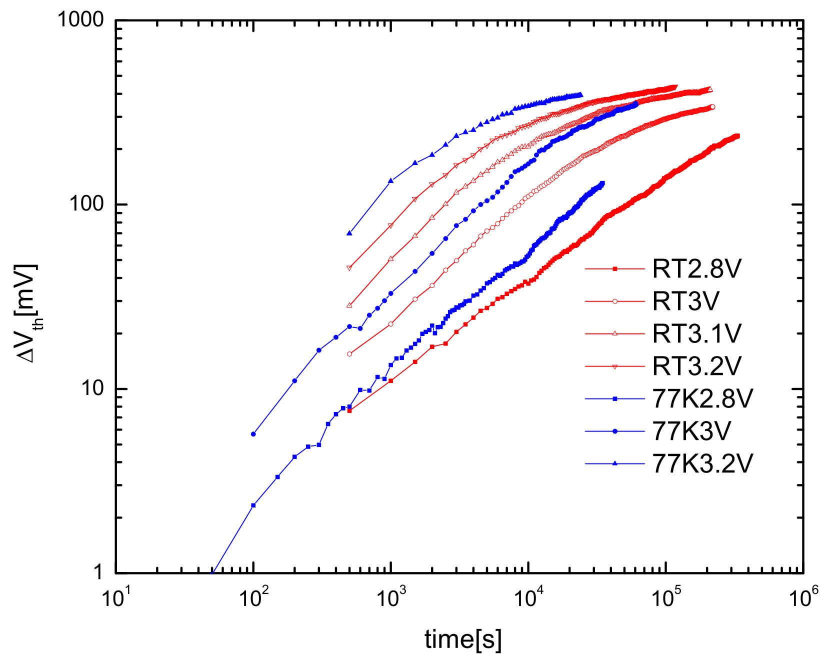


Figure 3.14: Degradation Results of the threshold voltage for NMOS devices with minimal length. The threshold voltage increases during hot carrier stress.

3.4.2 Subthreshold Swing

Figure 3.15 shows how the subthreshold swing changes after hot carrier stress at both 300K and 77K.

Subthreshold swing is calculated by linear fitting $log_{10}I_{ds}$ verse V_{gs} in the subthreshold region of the device. The reciprocal of the slop is the subthreshold swing. The degradation of

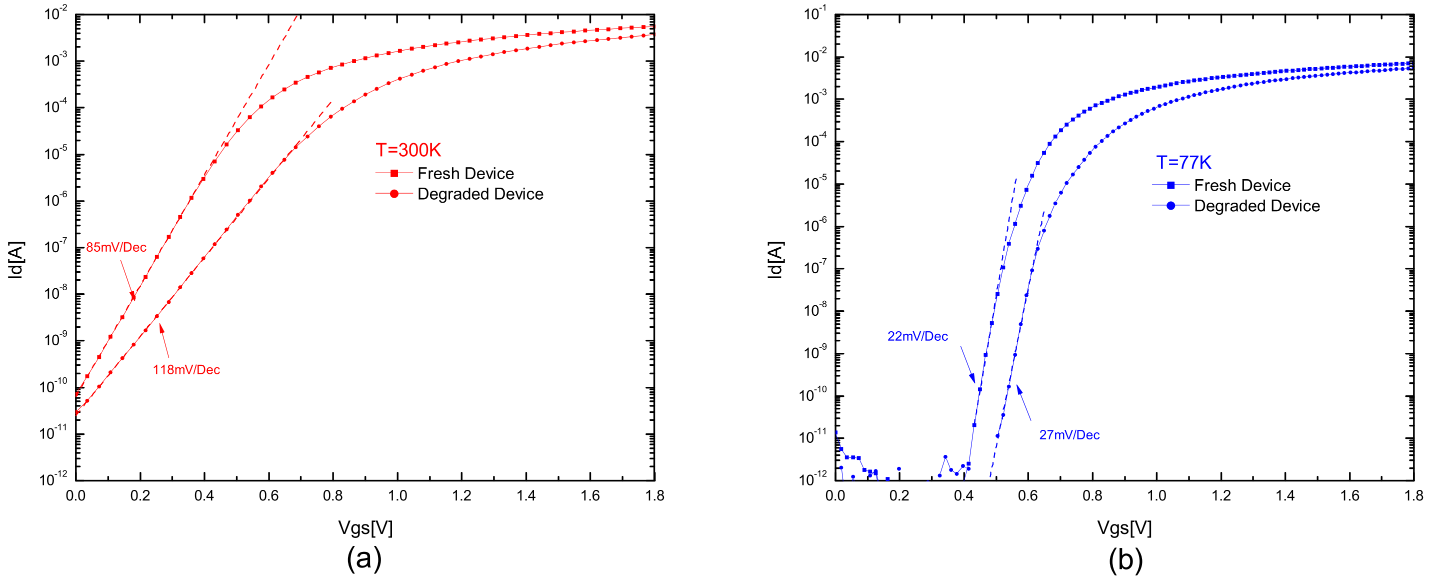


Figure 3.15: Subthreshold swing of the fresh and degraded NMOS device with minimal length at (a)300K and (b)77K

subthreshold swing during HCE at 300K is shown in Figure 3.16. The subthreshold swing at 300K increases during HCE as expected.

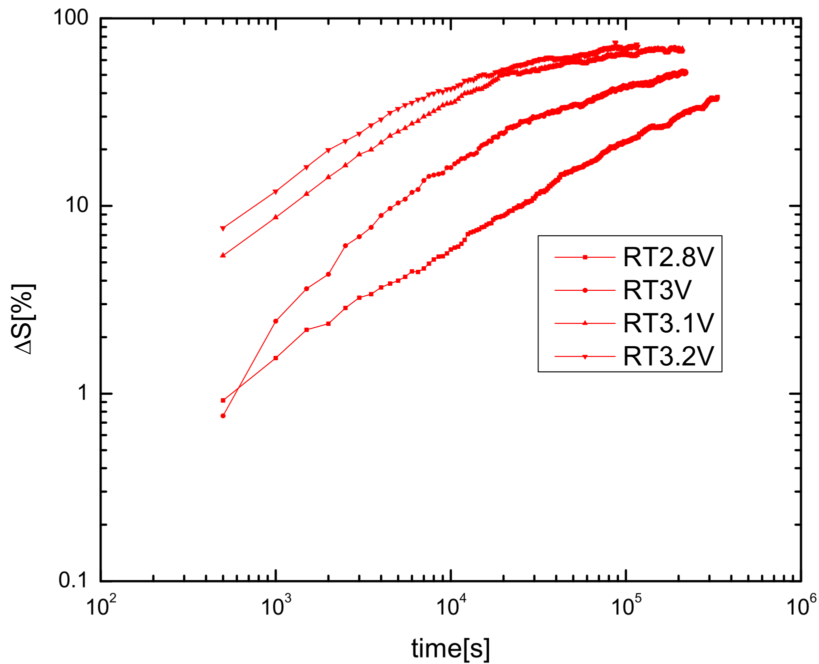


Figure 3.16: Degradation of subthreshold swing during HCE at 300K.

The degradation of subthreshold swing at 77K is shown in Figure 3.17. The limited quality of the measurement might be due to a less stable connection between the DUT and the channel of the analyzer than that at 300K due to the generating of bubbles (Nitrogen) because of heat

at the contact surface. These measurements are much worse due to the extremely low current. Nonetheless the increase of subthreshold swing at 77K is still evident.

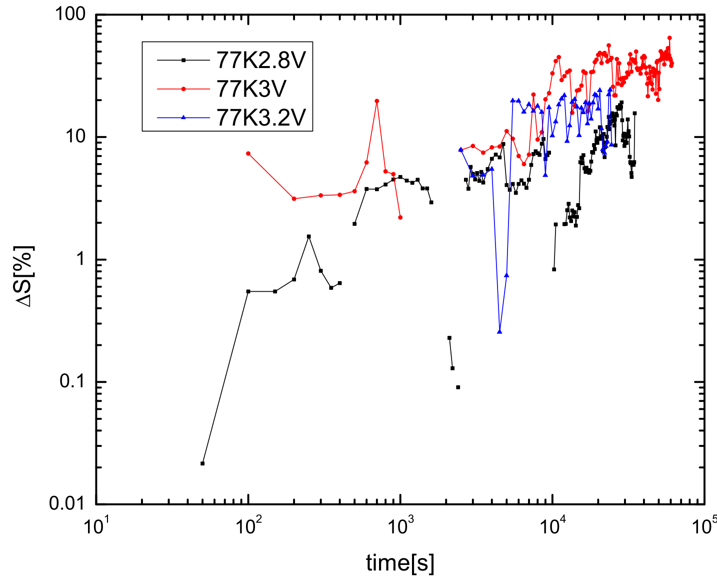


Figure 3.17: Degradation of subthreshold swing for NMOS devices with minimal length during HCE at 77K.

3.4.3 Mobility

The slope of the fitting lines in the saturation region in Figure 3.13 demonstrates the mobility degrades after hot carrier stress. The lower slope represents the lower mobility. To calculate the mobility degradation, we perform linear fitting on $\sqrt{I_{ds}}$ verse V_{gs} at saturation region. The slope of the fitting function is $\sqrt{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}}$. Mobility can thus be calculated. The degradation of mobility for NMOS devices with minimal length during HCE is shown in Figure 3.18.

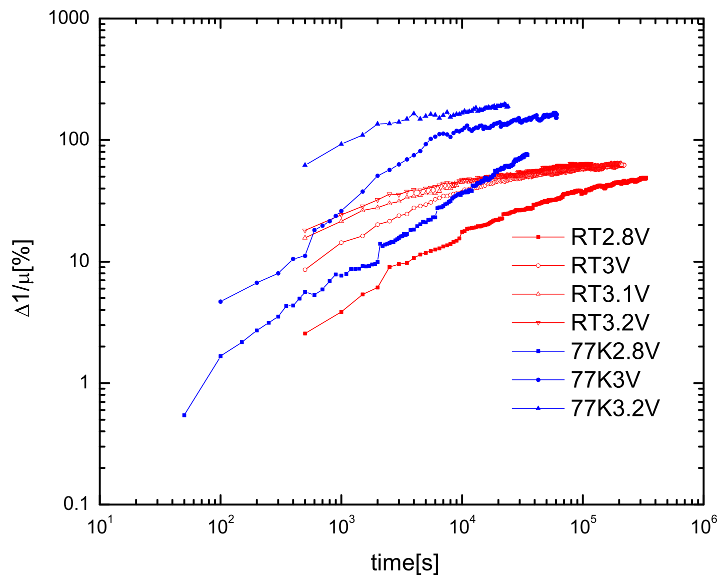


Figure 3.18: The degradation of mobility for NMOS devices with minimal length during hot carrier stress.

Chapter 4

Hot Carrier Induced Low-Frequency Noise Degradation

Low noise performance is critical in the front-end ASIC for LAr TPC. Hot carrier stress can induce an increase of low-frequency noise of MOSFETs [40–44] and this will affect the resolution of the front-end electronics [10]. Consequently, it becomes necessary to evaluate the low-frequency noise degradation for the adopted CMOS process from hot carrier stress. In this chapter, background information about noise is firstly introduced. Measurement setup is then discussed. Approaches to minimize the noise floor in noise measurements are covered. Results of noise degradation during hot carrier effect are analyzed in the last section.

4.1 Background of Noise

Noise presents as a random fluctuation of voltage or current, and it is superposed to a signal of interest. It can be either picked up from the environment or generated internally in active devices. Normally, an actual signal can be written in the following form when noise is considered [21]

$$i(t) = I + i_n(t) \tag{4.1}$$

where $i(t)$ is the real signal, I is the ideal signal without noise and $i_n(t)$ is the noise component. As noise is random and unpredictable, it is always evaluated in average, in the form of mean square ($\overline{i_n^2(t)}$) or root mean square ($\sqrt{\overline{i_n^2(t)}}$).

A most commonly adopted method to analyze noise is to evaluate it in the frequency domain. In a narrow frequency interval (Δf approaches to zero), the ratio of the mean square value of the noise to the frequency interval is called the Power Spectral Density (PSD) of the noise at that frequency, denoted as $S_i(f)$ with the unit of A^2/Hz for currents or $S_v(f)$ with the unit of V^2/Hz for voltages [21]. The whole curve of PSD can be measured by sweeping the frequency interval in the desired range. The total noise power can be obtained by integrating the PSD of the noise following the expression [21]:

$$\overline{i_n^2(t)} = \int_0^\infty S_i(f)df \tag{4.2}$$

Often, the square root of PSD $\sqrt{S_i(f)}$ is used with the unit of $A/\sqrt{Hz}$ for currents or $V/\sqrt{Hz}$ for voltages.

In frequency domain, if the PSD of a noise source is independent of frequency, we will call it white noise. It will be a flat line in the PSD curve as shown in Figure 4.1. Strictly speaking, white noise does not exist because in that case, the total noise power will be infinite. But if the PSD of a noise source is independent of frequency in the interested frequency region, we will still treat it as white noise.

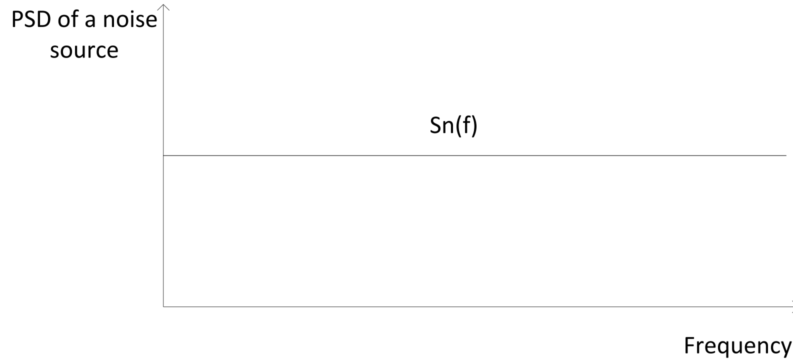


Figure 4.1: PSD of white noise

Noise can be treated in the same way as signal but must be used in the power form. Therefore, for a MOSFET, the noise voltage source at the gate terminal is equivalent to a noise current source between drain and source terminal as shown in Figure 4.2 with the following equation

$$S_i = S_v \times g_m^2. \tag{4.3}$$

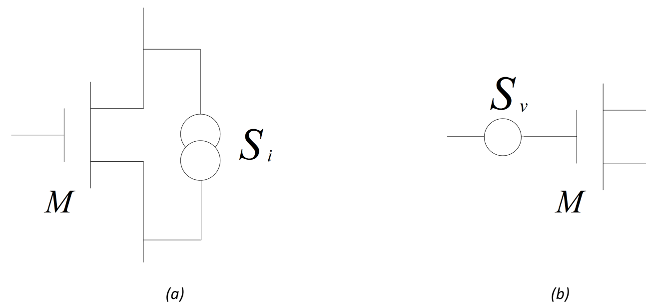


Figure 4.2: Noise equivalent in MOSFET

For a transistor, thermal noise, shot noise and low-frequency noise are the main types of noise. We will provide some general background of these noise sources in the following section.

4.1.1 Thermal Noise

Thermal Noise (also called Johnson noise, Nyquist noise) is due to the random thermal motion of the carrier in conductors above 0K [21]. For resistor, thermal noise can be modeled as a voltage source in series with a noiseless resistor of the same value as shown in Figure 4.3 (a) with the PSD of [21]

$$S_{vR,t} = 4kTR \tag{4.4}$$

In saturation region, where all transistors in our design operate, thermal noise of MOSFET can be modeled as a current source in parallel with the MOSFET as shown in Figure 4.3(b). The noise source can be expressed as [45]

$$S_{iM,t} = 4kT\gamma g_{ms} \tag{4.5}$$

where γ is a constant and g_{ms} is the source transconductance. For long channel device, γ can be determined to be $\frac{2}{3}$. It might be larger for submicron devices.

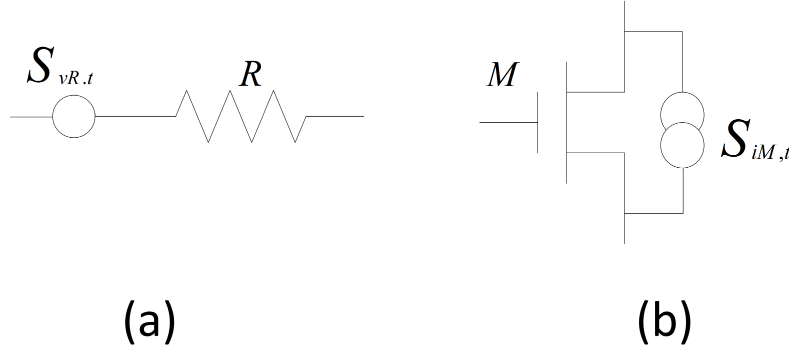


Figure 4.3: The model of thermal noise for (a)resistor and (b)MOSFET

4.1.2 Shot Noise

The current flow in devices is not a continuous flow but instead the sum of discrete pulses occurring randomly in time [10, 46] which leads to statistical fluctuation of the current [47]. The noise due to the current fluctuation is shot noise which is white and temperature independent [47]. In the case of potential barrier like p-n junction, where carriers can be treated as independent of each other [47, 48], shot noise is modeled as a current source in parallel of the device with the PSD of [10, 47]

$$S_{i,s} = 2qI \tag{4.6}$$

where $S_{i,s}$ is the PSD of shot noise, q is the charge of a carrier, I is the current flow over the device. Shot noise in the case of metallic conductor is far smaller due to the long-range correlations between charge carriers and is commonly ignored [47].

For MOSFET, the shot noise exists when it operates in subthreshold region [49]. As none of our MOSFETs are working in that region, shot noise will not be considered.

4.1.3 Low-frequency Noise

Low-frequency noise ($1/f$ noise, flicker noise) can be modeled as a current source in parallel with the MOSFET and is usually transformed to the voltage form in series with the gate terminal alone with the white term. It is believed to be originated from the fluctuation of the conductivity σ which has the form of $\sigma = q\mu n$ [50]. But whether it is the carrier number fluctuation or mobility fluctuation has been debated for several decades [21, 51, 52]. Here we will briefly introduce the basic idea of these two schools of thoughts.

Carrier Number Fluctuation Model

Carrier number fluctuation model, also called Mcwhorter Model, claims that low-frequency noise is caused by the random fluctuation of the number of carriers in the channel [51]. Traps in the silicon-oxide are responsible for this fluctuation by randomly capturing and releasing carriers through tunneling. The dynamic exchange of carriers between oxide traps and channel leads to a fluctuation of total oxide charges ΔQ_0 thus resulting in a fluctuation of threshold voltage according to Equation 2.11 by changing the flatband voltage. Hot carrier effect is known to raise low-frequency noise significantly [40–44]. The induced interface states by hot carrier injection have similar effects as those intrinsic traps [15]. Some researchers claim that interface states state cannot cause low-frequency noise directly as the capturing and releasing time of interface states are too short [53] or can only contribute to the low-frequency noise in the higher frequency range (higher than 1KHz) [40]. Other researchers have shown low-frequency noise at 15Hz brought up by hot carrier induced interface states [54]. Also our experiments show the increase of low-frequency noise in the full range from 10Hz to 50MHz.

The spectrum of noise raised up by a certain trap can be described by the following equation [51]

$$S_{LS} = \frac{q^2}{W^2 L^2} 4\overline{\Delta N_{OX}^2} \frac{\tau}{1 + (2\pi f \tau)^2} \tag{4.7}$$

where N_{OX} is the number of oxide charges due to the trap and τ is the time constant of the trap. This spectrum is usually called Lorentizan Spectrum which has been reported in the literature [55, 56] as well as some of our tested devices. The superposition of traps with different time constants will give us a normally seen 1/f spectrum [51] like shown in Figure 4.4

In carrier number fluctuation model, low-frequency noise can be expressed as the following [21]

$$S_{v,fN} = \frac{K_f}{C_{ox}^2 W L f^{AF}} \tag{4.8}$$

where K_f is a constant that depends on process with a typical value from $5 \times 10^{-31} C^2 cm^{-2}$ to $1 \times 10^{-30} C^2 cm^{-2}$, AF is a constant depends on process with value between 0.7 and 1.2.

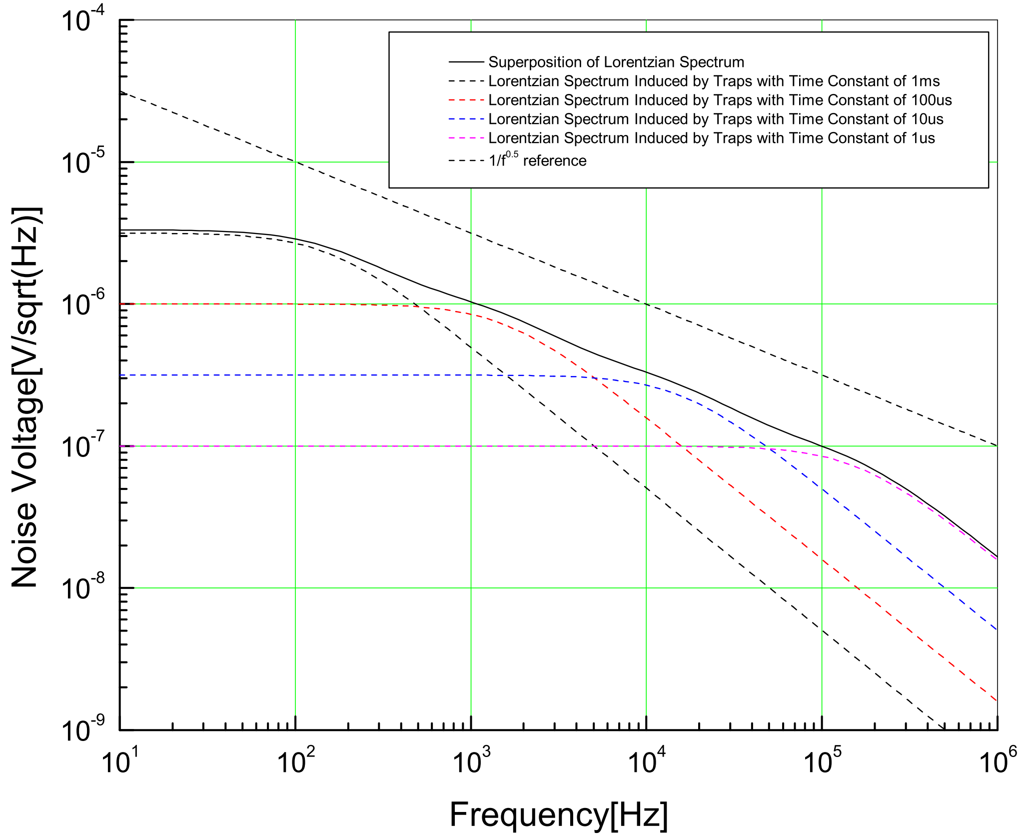


Figure 4.4: Superposition of Lorentzian Components induced by traps with time constant of $1ms$, $100\mu s$, $10\mu s$ and $1\mu s$.

Mobility Fluctuation Model

The mobility fluctuation model, also called Hooge model, is based on the empirical equation [50, 51, 57, 58]

$$\frac{S_I(f)}{I^2} = \frac{S_\mu(f)}{\mu^2} = \frac{\alpha_H}{fN} \tag{4.9}$$

where $S_x(f)$ is the spectral density with fluctuations of the quantity x, α_H is a constant depends on technology and N is the total number of carriers. The equation is based on experimental observations in homogeneous layer and has no physical theory behind [57, 58]. In this model, low-frequency noise can be expressed as [21]

$$S_{v,fM} = \frac{K(V_{gs})}{C_{ox}WLf} \tag{4.10}$$

where $K(V_{gs})$ is a bias dependent quantity with a typical value from $6 \times 10^{-26}V^2F$ to $2 \times 10^{-23}V^2F$.

Application of the Two Models

Both of the two models have their own supporting research. Some researchers [21, 51, 58] believe that Mcwhorter's model is more suitable for NMOS while Hooge's model find better

agreement in PMOS. Some other researchers [59] proposed a unified model that combines both Mcwhorter's model and Hooge's model by attributing mobility fluctuation to the coulomb scattering of the fluctuating oxide charge in the number fluctuation model. This model is used in Berkeley Short Channel IGFET (BSIM) and is widely adopted for simulation [51].

4.1.4 Noise Modeling in Circuits

Noise Correlation

Noise sources can be either correlated or non-correlated. Figure 4.5 shows these two different cases.

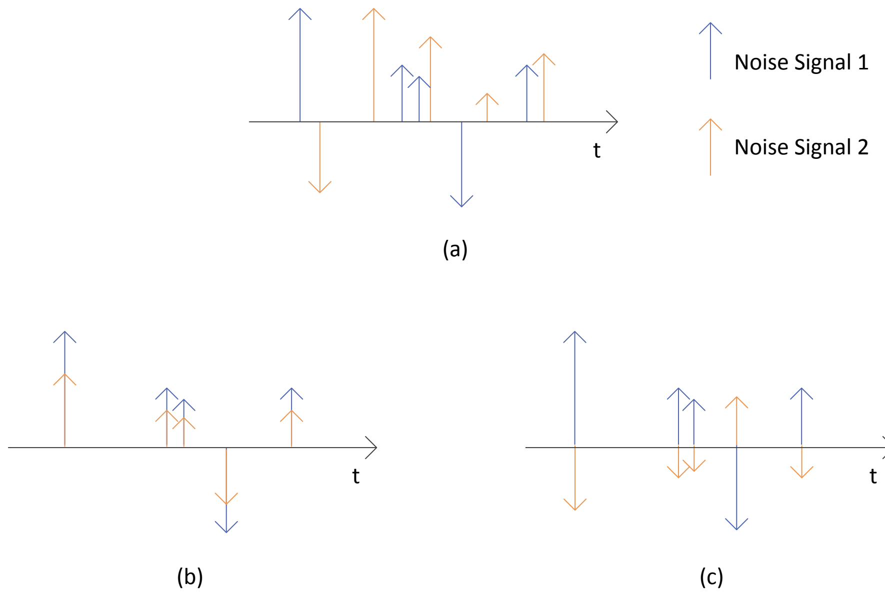


Figure 4.5: The blue and yellow arrow represent pulses from different noise sources. $(a), (b), (c)$ shows the case that they are non-correlated, fully-correlated and anti-correlated respectively.

When considering the PSD of the total noise, the following equation can be used [10]

$$S_{total} = S_1 + S_2 + CS_1S_2 \tag{4.11}$$

where S_{total} is the PSD of the total noise, S_1 and S_2 are the PSD of noise source 1 and 2 respectively and C is the correlated coefficient ranging from -1(when two noise sources are anti-correlated, e.g. identical in amplitude but reverse in phase) to 1 (when noise source 1 and 2 are fully-correlated). For non-correlated noise sources, C=0 and we can add up the PSD directly as

$$S_{total} = S_1 + S_2 \tag{4.12}$$

In most cases, noise sources are non-correlated. For example, the thermal noise and low-frequency noise of the same transistor are non-correlated and noise from different devices are also non-correlated [21, 60]. Noises sources in this chapter will be non-correlated unless specified.

Norton-Thevenin Equivalent

Norton-Thevenin Equivalent is important for noise analysis. Let's take a noisy resistor for example. A resistor can be modeled as an ideal resistor of same resistance in series with a noise voltage source (Thevenin Form) as shown in Figure 4.6(a) or transformed into Norton form as shown in 4.6(b), with

$$S_v = S_i \times R^2. \tag{4.13}$$

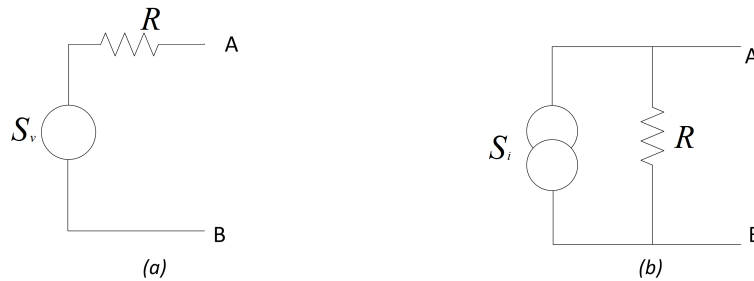


Figure 4.6: (a) and (b) represent the noise equivalent of a noisy resistor in Thevenin form and Norton form respectively.

Blakesley's Transformation

Blakeley's Transformation describes the shift of current and voltage source through nodes. In the current form, a current source between node A and B can be replaced by two current sources with the same value and polarity between node A, B and an additional node C in the middle as shown in Figure 4.7 (a). Figure 4.7 (b) exhibits the voltage form in which the voltage source can be shifted through node A into each branch. The generated voltage sources on each branch have the same value and polarity with the original one. In both current and voltage form of Blakesley's Transformation, the newly generated sources after transformation are fully correlated with each other.

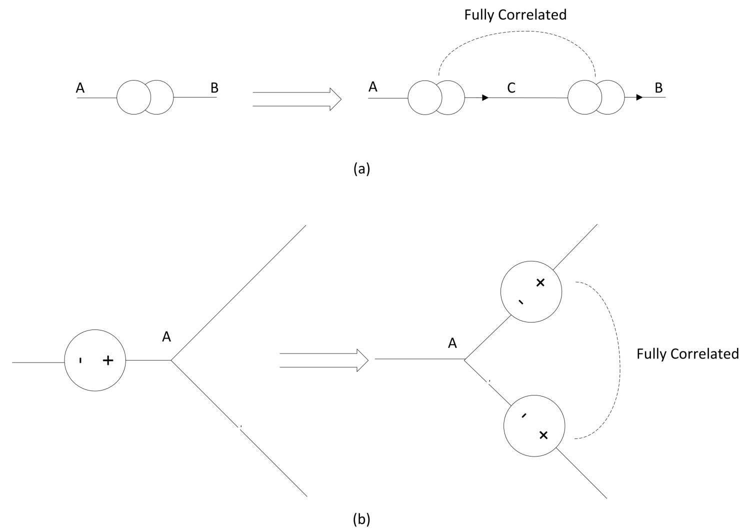


Figure 4.7: Blakesley Transformation in (a) current form, (b) voltage form.

Equivalent Input Noise

Figure 4.8 presents the case that a noise source ($\overline{v_{n,in}^2}$) and a signal source ($v_{s,in}$) placed at the input terminal of an ideal amplifier. At the output terminal, noise as well as signal are amplified by the gain of amplifier (Av) to be $A_v^2 \times \overline{v_{n,in}^2}$ and $A_v \times v_{s,in}$, respectively.

Signal to Noise Ratio (SNR) is defined as the ratio of the signal power to noise power [61] thus represents the performance of a system. In the above example, even though after the amplifier the noise is increased we cannot simply get the conclusion that after amplification the noise performance got worse as the SNR keeps the same.

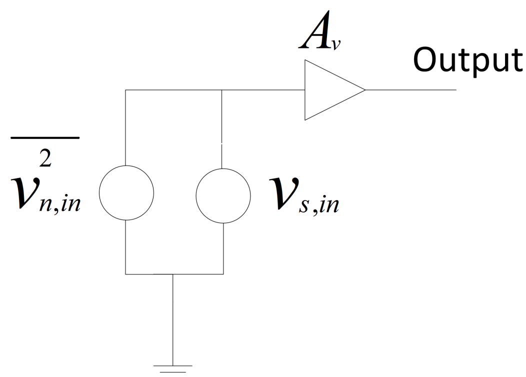


Figure 4.8: Noise source and signal source followed by an ideal amplifier.

The concept of equivalent input noise is therefore introduced and is widely adopted to represent all the noise sources of a system. It is composed of a noise voltage and a noise current placed at the input terminal. A noisy circuit can be modeled as shown in Figure 4.9(a) [60].

Both noise voltage $S_{v,in}$ and noise current $S_{i,in}$ contribute partially to the output noise. In order to determine their value, the input terminal is set to short and open respectively. Output

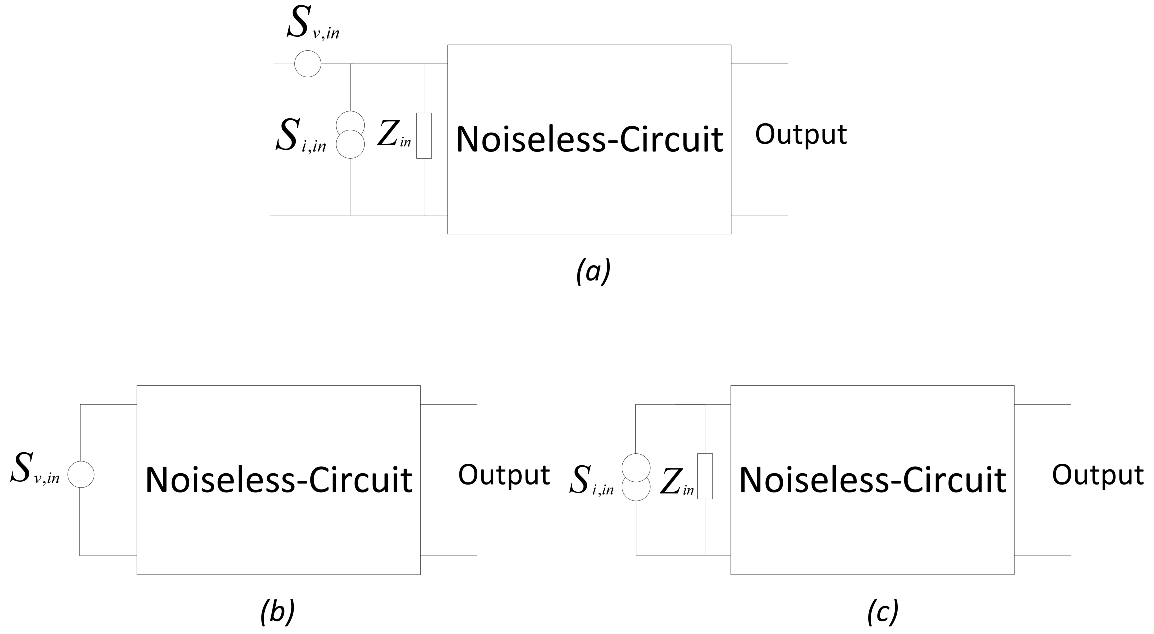


Figure 4.9: (a)Equivalent input noise model for circuits. (b) Short the input terminal to calculate $S_{v,in}$. (c) Open the input terminal to calculate $S_{i,in}$.

noise can be then calculated or measured. We could get the equivalent input noise voltage as

$$S_{v,in} = \frac{S_{vshort,out}}{|A_v(f)|^2} \tag{4.14}$$

and equivalent input noise current as

$$S_{i,in} = \frac{S_{vopen,out}}{|A_v(f)|^2 * |Z_{in}|^2} \tag{4.15}$$

where $S_{v,in}$ and $S_{i,in}$ represent the PSD of equivalent input noise voltage and current respectively, $S_{vopen,out}$ and $S_{vshort,out}$ is the PSD of output noise voltage when input terminal is open and short respectively, $A_v(f)$ is the voltage gain and Z_{in} is the input impedance. The connection of input terminal to get the noise voltage and noise current can be explained as the following. When the input terminal is short, $S_{i,in}$ will flow through the short path without influencing the circuit. The output noise will be then determined only by the noise voltage. Similarly, when the input terminal is opened, only noise current will contribute to the output noise.

For a MOSFET operates in strong inversion, two major non-correlated noise sources exist: low-frequency noise and thermal noise. From Equation 4.3 and 4.5, thermal noise can be represented as a voltage source at the gate terminal with the expression of

$$S_{v,w} = \frac{4kT\gamma g_{ms}}{g_m^2} = \frac{4kT\gamma n}{gm} \tag{4.16}$$

where n is defines as $n = \frac{g_{ms}}{g_m}$ with a typical range of $1.1 < n < 1.6$ [62].

The two non-correlated noise sources composed equivalent input noise can be expressed as

$$S_{v,in} = S_{v,w} + S_{v,f} = \frac{4kT\gamma n}{gm} + \frac{K_1}{C_{ox}^2 W L f^{AF}} \tag{4.17}$$

Figure 4.10 shows the equivalent input noise of a MOSFET. Low-frequency noise dominates the low frequency range. The PSD of the low frequency noise goes down with the frequency increases. After Corner Frequency where the contribution from the two noise sources is equal, thermal noise will be the major part.

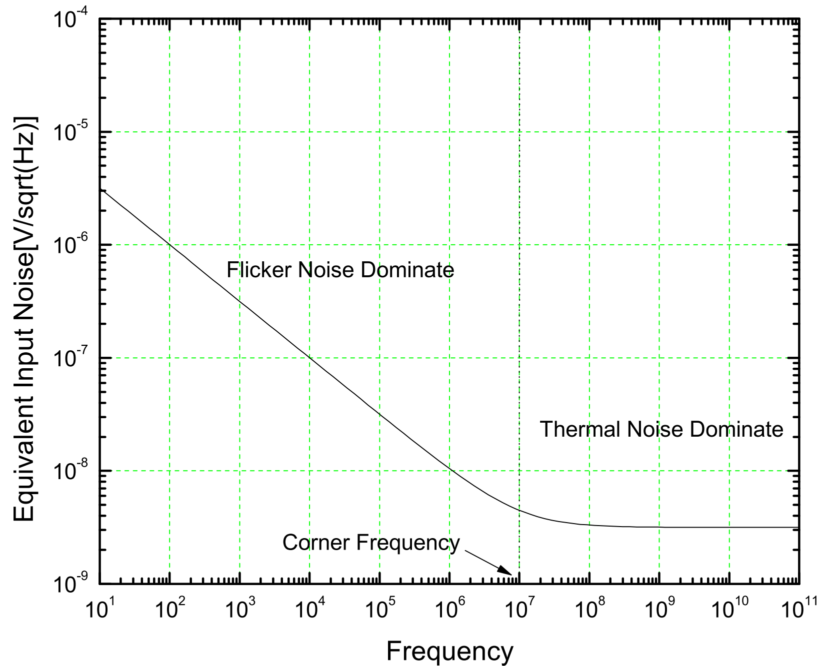


Figure 4.10: Equivalent input noise of a MOSFET

4.2 Test Setup for Noise Measurement

Noise measurement is the key part of studying hot carrier induced noise degradation. The basic idea is to separate the noise of DUT from the noise of other devices, measurement instruments and the environment. Proper amplification of the noise from DUT, shielding, filtering and ground loop reduction are critical. In this section, the test setup and important methods to eliminate irrelevant noise sources are introduced. We are able to show the PSD of the DUT from 10Hz up to 50MHz (40MHz for PMOS) at both 300K and 77K. The DUT is the same MOSFET as used in the transistor lifetime test (TSMC $0.18\mu m$ CMOS process with $W = 5 \times 2\mu m, L = 180nm$).

4.2.1 Schematic of Test Setup

We use the test setup for noise measurement of NMOS as an example. The case for PMOS will be similar. The schematic of the setup is shown in Figure 4.11 which is designed to operate at

both 300K and 77K.

In this setup, three amplification stages are used. Stage 1 is a common source amplifier realized using the DUT (M1) which becomes the input transistor of our setup. Stage 2 is a NPN emitter degenerated common emitter bipolar circuit. Next, we use the lower-noise amplifier integrated in our oscilloscope Tektronix TDS784D. These three amplification stages provide a DC gain of about 10, 4 and 10 respectively. Low-noise buffers are added at the output of amplification stages 1 and 2 to provide better drive capability. All components are discrete.

Amplification stage 1 and buffer stage 1 are made on a dedicated printed-circuit board (PCB) designed to operate at both 77K and 300K. As BJT's performance will severely degrade in cryogenic environment (current gain might decrease 2 to 3 orders of magnitude from 300K to 77K [63]), the BJT part is realized as a separate circuit and will be kept at 300K. Agilent 4395A is used as the spectral/network analyzer. We selected low-noise power supplies E3610A, E3614A, 6114A from HP to provide the required voltages.

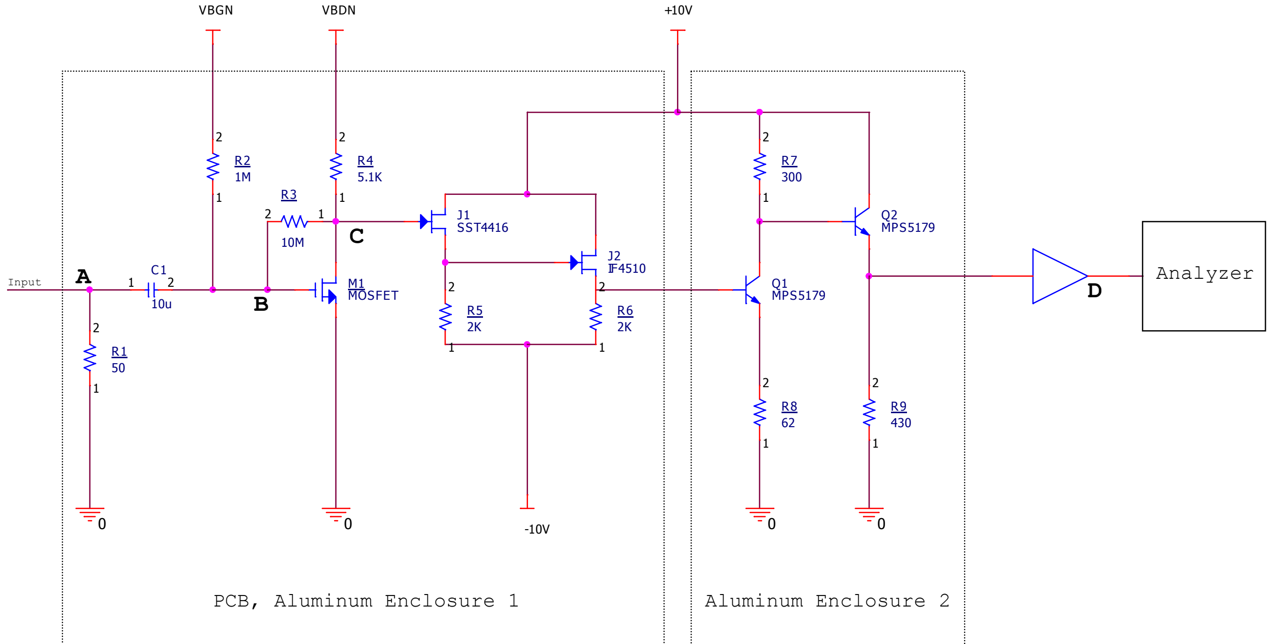


Figure 4.11: Schematic of the noise measurement system for NMOS

In our system, the equivalent input voltage noise of the system $(S_{v,in})$ is the same as that of the DUT (M1) which will be explained in the next sub-section. We need to measure the PSD of output noise $(S_{v,out})$ when input terminal is short to ground as well as the transfer function of the circuit $(A_v(f))$. In this way we can get

$$S_{v,in} = \frac{S_{v,out}}{|A_v(f)|^2} \tag{4.18}$$

When measuring $S_{v,out}$, the input terminal is grounded and the output terminal is connected to the spectral analyzer. For the measurement of $A_v(f)$, the network mode of the analyzer is used. As the signal might be saturated during amplification, proper attenuation needs to be selected.

The capacitance at the drain terminal of the MOSFET is important for noise measurements as it will limit the bandwidth of amplification stage 1, resulting a lower amplification of the noise from M_1 after the cut off frequency. Therefore we want to minimize that. The capacitance at the drain terminal is composed of three parts: parasitic capacitance, capacitance from MOSFET (gate-drain capacitance, drain-bulk capacitance, etc) and capacitance from the following JEFT (gate-drain capacitance, gate-source capacitance, etc.). The capacitance from the MOSFET is a characteristic of the device which can hardly be changed during the test. To minimize the total capacitance at the drain terminal we choose a low capacitance JFET as the source follower. To reduce the parasitic capacitance, we use the unpackaged die and connect the device to the PCB pad directly with wirebond as shown in Figure 4.12.

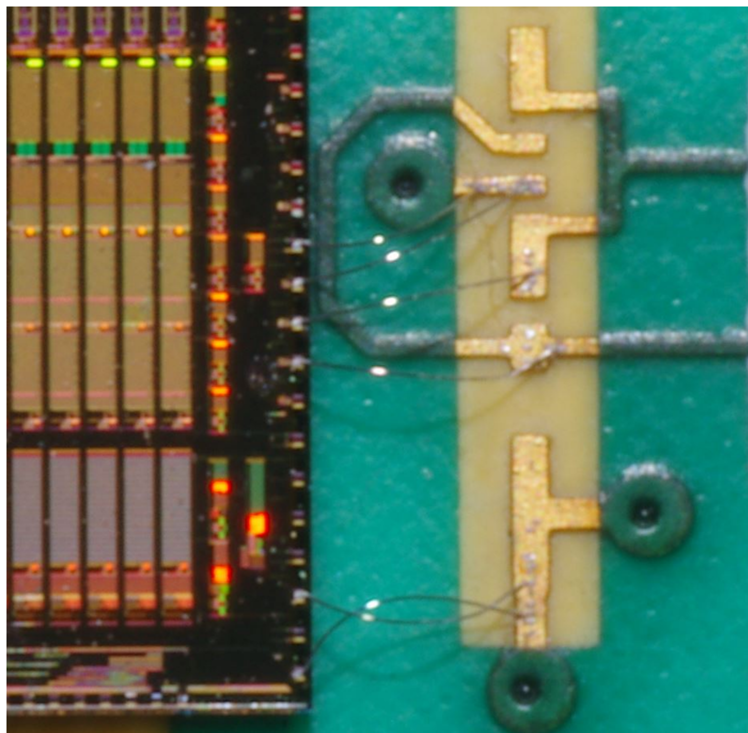


Figure 4.12: Wirebond to reduce parasitic capacitance.

Both noise measurement and hot carrier stress are performed using the same PCB. To get coherent result, the bias point of the DUT is set the same as the one used in Chapter 4. At room temperature, noise of the fresh device is firstly measured with operating point: $V_{ds} = V_{gs} = 1V$. The drain current is measured to be 1.8mA in this condition. Then stress is performed for the device with the condition of $V_{ds} = 3.2V, I_d = 2.4mA$. As the threshold voltage will increase during hot carrier stress, we need to keep increasing the gate-source voltage to keep the drain current unchanged. After the device reaches 10% degradation in transconductance, noise is measured again. This time, for the noise measurement, the drain-source voltage is still keep at 1V while the gate-source voltage is increased to keep the drain current at 1.8mA. Each noise measurement takes 30 times average for reliable results.

Figure 4.13 shows the whole setup of the noise measurement.

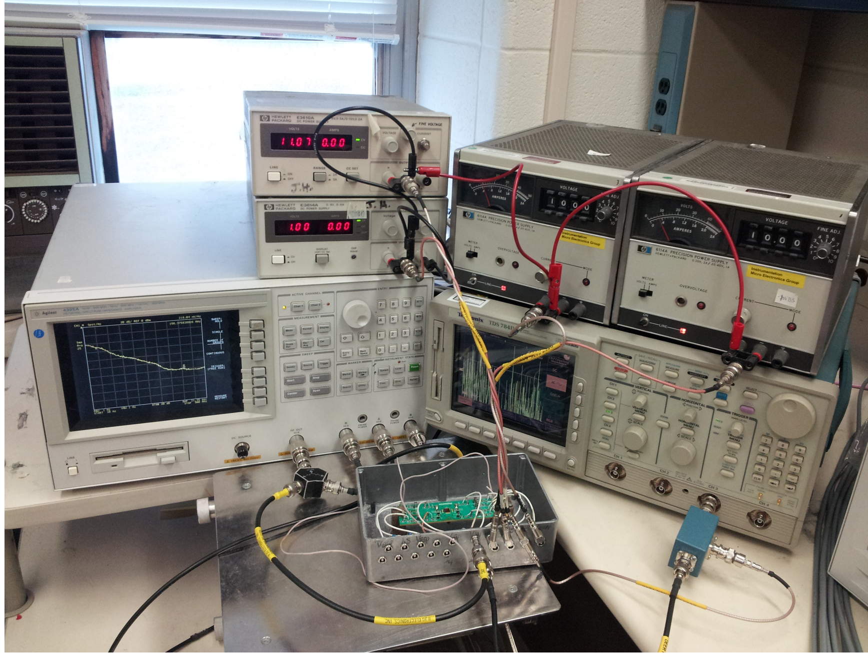


Figure 4.13: Equipments for the noise measurement.

4.2.2 Noise Source Analysis of the system

The contribution of noise sources from later stages to $S_{v,in}$ is reduced by the gain of its earlier stages therefore will be much smaller comparing with the noise of the DUT. These noise sources can be considered as part of the noise floor. We will only evaluate noise sources from devices in the first stage. Let's start with the noise from all resistors. When measuring noise, the input terminal (Node A) is shorted to ground. Therefore, noise from R_1 will not contribute. Noise sources from R_2, R_3, R_4 are shown in Figure 4.14 with

$$S_{i,R_2} = \frac{4kT}{R_2}, S_{i,R_3} = \frac{4kT}{R_3}, S_{i,R_4} = \frac{4kT}{R_4}. \tag{4.19}$$

Applying current form of Blakesley's transformation, the current noise source S_{i,R_3} from R_3

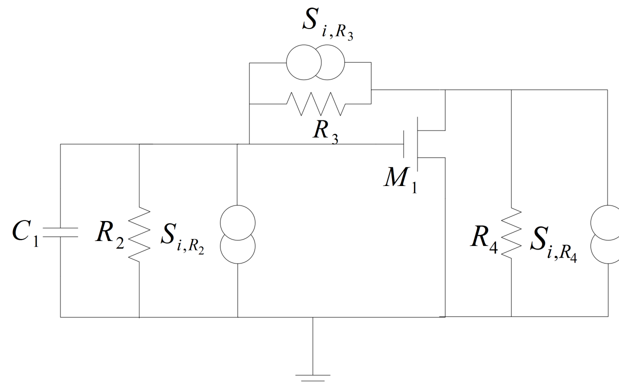


Figure 4.14:

can be split into two fully correlated current sources (marked with $*$ in the schematic) with an

additional ground node in the middle. We have

$$S^{''}_{i,R_3} = S^{'}_{i,R_3} = S_{i,R_3} = \frac{4kT}{R_3} \tag{4.20}$$

These two sources could be moved to the input and out of the transistor M_1 respectively as shown in Figure 4.15.

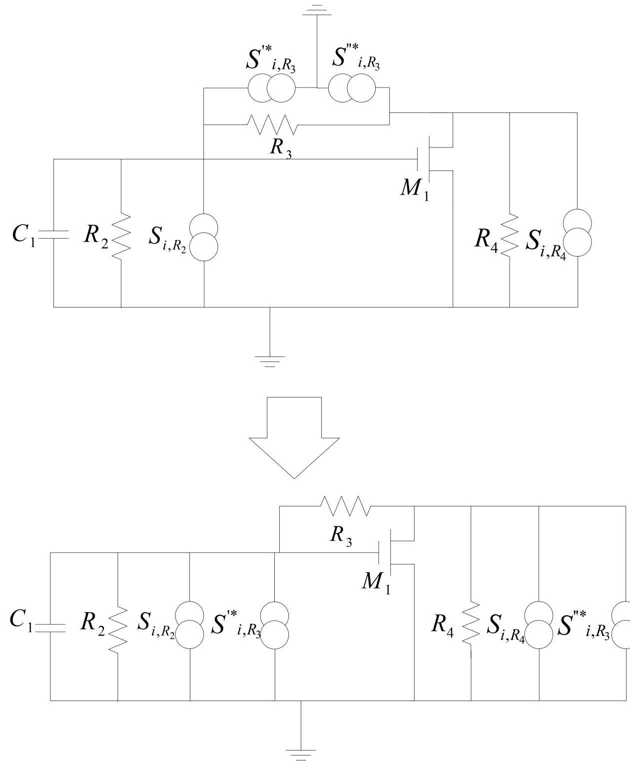


Figure 4.15:

Noise source from transistor M_1 is shown in Figure 4.16. S_{vM_1} is the noise of the transistor which is described in Equation 4.17. Using the voltage form of Blakesley's transformation, S_{vM_1} can be substituted by the fully correlated source $S^{'}_{vM_1}$ and $S^{''}_{vM_1}$ (marked with $\circ$ in the schematic) as shown in Figure 4.17. $S^{'}_{vM_1}$ and $S^{''}_{vM_1}$ can be transferred to current form $S^{'}_{iM_1}$

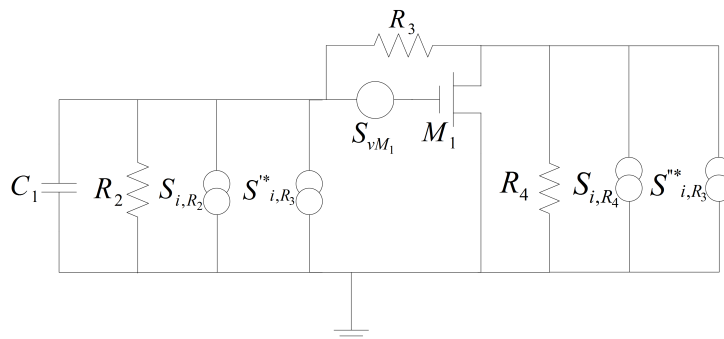


Figure 4.16:

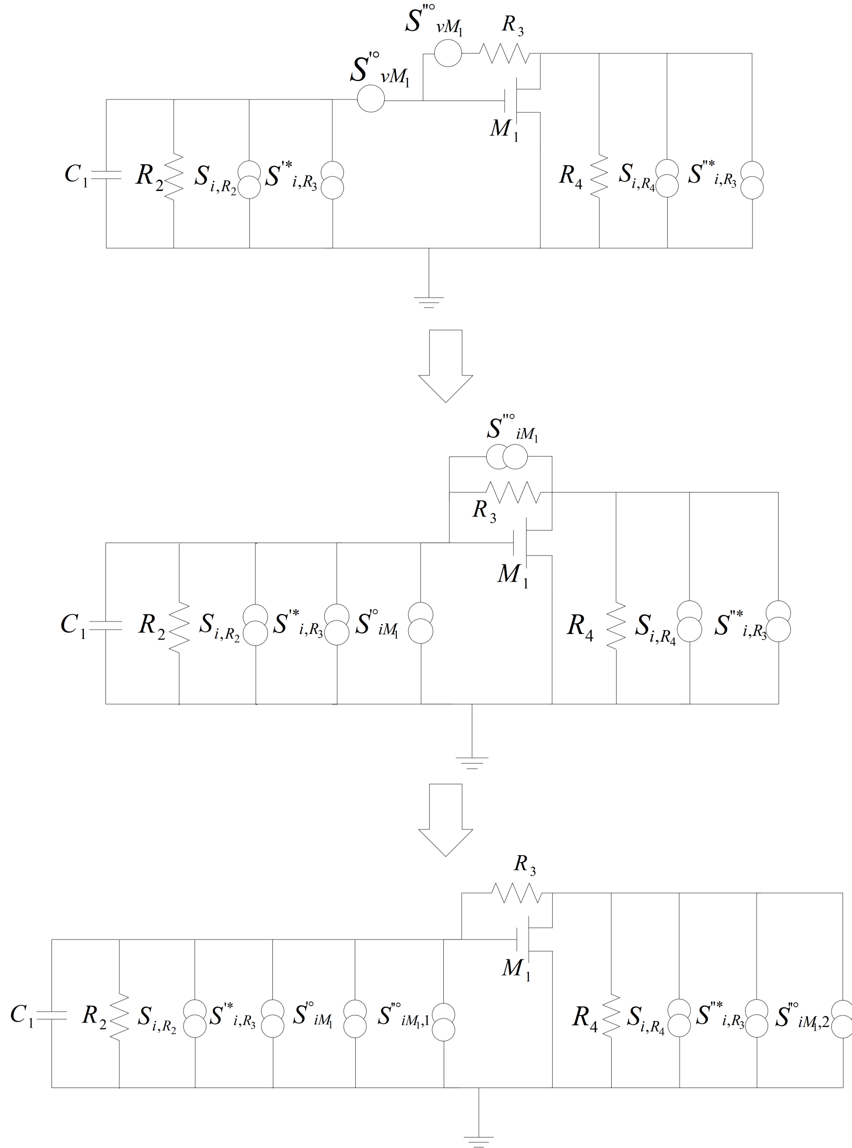


Figure 4.17:

and $S^{''}_{iM_1}$ respectively using Norton-Thevenin Equivalent. We have

$$S^{'}_{iM_1} = \frac{S^{'}_{vM_1}}{|\frac{1}{C_1 s}//R_2|^2} = \frac{S_{vM_1}}{|\frac{1}{C_1 s}//R_2|^2} \tag{4.21}$$

$$S^{''}_{iM_1} = \frac{S^{''}_{vM_1}}{R_3^2} = \frac{S_{vM_1}}{R_3^2} \tag{4.22}$$

As the minimum frequency of the analyzer is 10Hz and R_2, R_3 is very large (1Mohm and 10 Mohm respectively). The impedance seen from node B in Figure 4.11 in the interested region (larger than 10Hz) is dominated by capacitor C_1

$$Z \approx \frac{1}{|C_1 s|} \tag{4.23}$$

Therefore

$$S^{'}_{iM_1} \approx |C_1 s|^2 * S_{vM_1} \tag{4.24}$$

$S^{''}_{iM_1}$ can be further substituted by $S^{''}_{iM_1,1}$ and $S^{''}_{iM_1,2}$ (fully correlated, marked with $\circ$ in the schematic) using the current form of Blakesley's transformation similarly with the processing of S_{i,R_3}. We have

$$S^{''}_{iM_1,1} = S^{''}_{iM_1,2} = S^{''}_{iM_1} = \frac{S_{vM_1}}{R_3^2}. \tag{4.25}$$

Now let's calculate combination of the four noise sources $S_{icombine,in}$ at the input terminal of M_1. $S^{'}_{iM_1}$ and $S^{''}_{iM1,1}$ are fully correlated while others are non-correlated. Therefore, we have

$$\begin{aligned} S_{icombine,in} &= S_{i,R_2} + S^{'}_{i,R_3} + (\sqrt{S^{'}_{iM_1}} + \sqrt{S^{''}_{iM_1,1}})^2 \\ &= S_{i,R_2} + S^{'}_{i,R_3} + S_{vM_1}(|C_1 s| + \frac{1}{R_3})^2 \\ &\approx S_{i,R_2} + S^{'}_{i,R_3} + S_{vM_1}(|C_1 s|)^2 \\ &= S_{i,R_2} + S^{'}_{i,R_3} + S_{vM_1}\frac{1}{Z^2} \end{aligned} \tag{4.26}$$

The transfer function of the circuit from node B to node C in Figure 4.11 can be expressed as

$$A_v = \frac{1 - R_3 g_m}{1 + \frac{R_3}{r_o//R_4}} \tag{4.27}$$

As R_3 is very large ($10M\Omega$), we have

$$A_v \approx -g_m(r_o//R_4) \tag{4.28}$$

Now refer $S_{icombine,in}$ to node C in Figure 4.11. $S_{vM_1} * \frac{1}{Z^2}$ is fully correlated with $S^{''}_{iM_1,2}$ and $S^{'}_{i,R3}$ is fully correlated with $S^{''}_{i,R_3}$. We have

$$\begin{aligned} S_{vtotal,out} = \Bigg[& \underbrace{S_{i,R_2} * Z^2 * g_m^2}_{1} + \underbrace{S_{i,R_4}}_{2} + \underbrace{\left(\sqrt{S^{'}_{i,R_3} * Z^2 * g_m^2} + \sqrt{S^{''}_{i,R_3}}\right)^2}_{3} \\ & + \underbrace{\left(\sqrt{S_{vM_1}\frac{1}{Z^2} * Z^2 * g_m^2} + \sqrt{S^{''}_{iM_1,2}}\right)^2}_{4} \Bigg] (r_o//R_4)^2 \end{aligned} \tag{4.29}$$

The frequency range of our analyzer is 10Hz-500MHz, g_m is around $4.7mS$ at 300K and $6.8mS$ at 77K. Terms in Equation 4.29, at 77K for example, can be calculated as the following

Term 1

$$\begin{aligned} S_{i,R_2} * Z^2 * g_m^2 &= \frac{4kT}{R_2} * \frac{1}{|C_1 s|^2} * g_m^2 \\ &\le \frac{1}{10^6 \times (10^{-5} \times 2\pi \times 10)^2}(6.8 \times 10^{-3})^2 \times 4kT(V^2/H_Z) \\ &= 1.2 \times 10^{-4} \times 4kT(V^2/H_Z) \end{aligned}$$

Term 2

$$S_{i,R_4} = \frac{4kT}{R_4} = \frac{1}{5.1\times 10^3} \times 4kT(V^2/H_Z) = 2\times 10^{-4} \times 4kT(V^2/H_Z)$$

Term 3

$$\begin{aligned}\left(\sqrt{S'_{i,R_3} * Z^2 * g_m^2} + \sqrt{S''_{i,R_3}}\right)^2 &= \frac{4kT}{R_3}\left(\sqrt{\frac{1}{|C_1 s|^2} * g_m^2} + 1\right)^2 \\ &\le \frac{1}{10^7}\left(\frac{1}{10^{-5}\times 2\pi \times 10} * 6.8\times 10^{-3} + 1\right)^2 \times 4kT(V^2/H_Z) \\ &= 1.4\times 10^{-5} \times 4kT(V^2/H_Z)\end{aligned}$$

Term 4

$$\begin{aligned}\left(\sqrt{S_{vM_1} * \frac{1}{Z^2} * Z^2 * g_m^2} + \sqrt{S''_{iM_1,2}}\right)^2 &= S_{vM_1}(g_m + \frac{1}{R_3})^2 \\ &\approx S_{vM_1} g_m^2 \\ &= 4kT\gamma n g_m + \frac{K_f * g_m^2}{C_{ox}^2 WLf^{AF}} \\ &> 1.1 \times \frac{2}{3} \times 6.8\times 10^{-3} \times 4kT + \frac{K_f * g_m^2}{C_{ox}^2 WLf^{AF}} \\ &= 5\times 10^{-3} \times 4kT + \frac{K_f * g_m^2}{C_{ox}^2 WLf^{AF}}\end{aligned}$$

From the above calculation, we can see that all noise sources from resistors are at least one order of magnitude smaller than the thermal noise from the MOSFET, thus can be ignored. Equation 4.29 is then changed to

$$S_{vtotal,out} = (4kT\gamma n g_m + \frac{K_f * g_m^2}{C_{ox}^2 WLf^{AF}})(r_o//R_4)^2 \tag{4.30}$$

Now, let's look at the measurement of transfer function in from Node A to D in Figure 4.11. Figure 4.18 shows the small signal model of the circuit for transfer function measurement. $-g_m(r_0//R_4)$ is the transfer function from node B to node C while H(s) refers to the transfer function from node C to node D. Therefore we have

$$|A_v| = \left|\frac{R_2}{\frac{1}{C_1 s} + R2}\right| * |-g_m(r_o//R_4)| * |H(s)| \tag{4.31}$$

When frequency of signal is higher than 10Hz, $\left|\frac{R_2}{\frac{1}{C_1 s}+R2}\right|$ approximates to 1, resulting

$$|A_v| \approx g_m(r_o//R_4) * |H(s)| \tag{4.32}$$

As the noise measured at the analyzer is $S_{vtotal,out} * |H(s)|^2$, the equivalent input noise of our setup can be derived as

$$S_{v,in} = \frac{S_{vtotal,out} * |H(s)|^2}{(g_m(r_o//R_4)|H(s)|)^2} = \frac{4kT\gamma n}{g_m} + \frac{K_f}{C_{ox}^2 WLf^c} \tag{4.33}$$

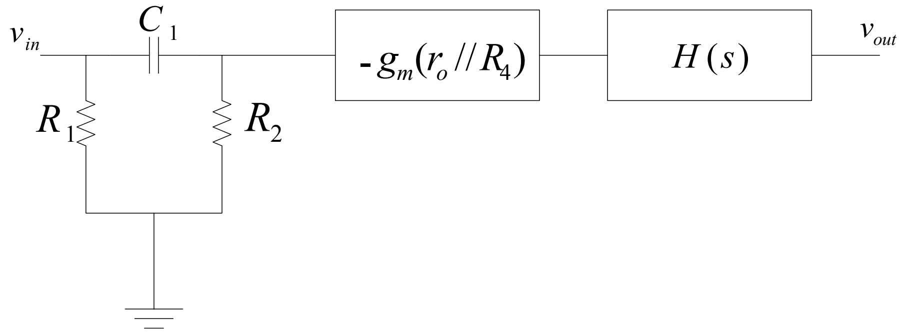


Figure 4.18: Small signal equivalent of test setup for transfer function measurement.

which is the same as the equivalent input noise of a single MOSFET. Therefore the measured equivalent input voltage noise of the system can treated as the equivalent input voltage noise of the DUT.

4.2.3 Minimize the Noise Floor

With the exception of noise sources from the DUT, any other noise source is treated as part of our noise floor. The components include the noise from voltage supplies, the noise from circuits and instruments at later stages, the noise from ground reference mismatch [64, 65] and the noise picked up from the environment. Minimizing the noise floor is essential for an accurate noise measurement. Here we will discuss the methods we adopted to achieve a low noise floor.

1. To reduce the noise coming from bias, we use low noise power supplies followed by low-pass filters. It is worth mentioning that stable batteries are better for noise measurement. The corner frequency of the filter is set below the minimum measurable frequency of the spectral analyzer (10Hz). Due to the parasitic inductance of the capacitor, non-ideal capacitors will have impedance curve as shown in Figure 4.19. In order to get a low impedance response in the whole frequency range, capacitors of different values are used in parallel.

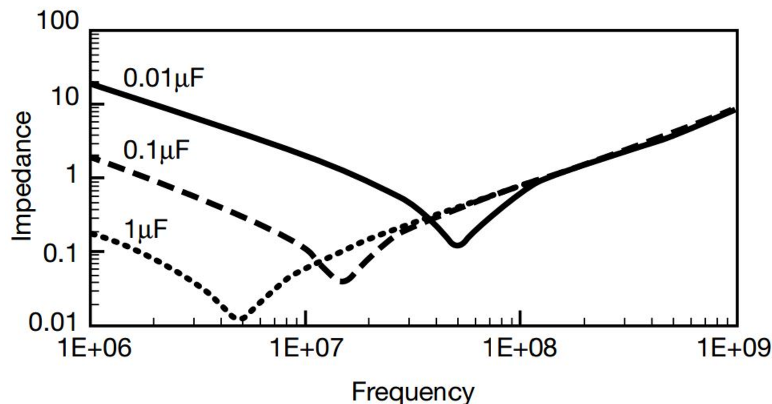


Figure 4.19: Impedance curve of commercial X7R ceramic capacitors of size 1206 [66].

2. Noise from later stages is reduced by the amplification. The DC gain of amplifier stage 1, 2 and 3 are around 10,4,10 respectively. Let's take the noise from the spectral analyzer as an example. The contribution of the noise from spectral analyzer to the equivalent input noise before any pole of the amplifiers can be expressed by

$$S_{vsa,in} = \frac{S_{v,sa}}{|A_{v1}A_{v2}A_{v3}|^2} = \frac{1}{1.6 \times 10^5} S_{v,sa} \tag{4.34}$$

where $S_{vsa,in}$ is the contribution of the noise from spectral analyzer to the equivalent input noise, $S_{v,sa}$ is the noise of the spectral analyzer, A_{v1}, A_{v2}, A_{v3} is the DC gain of amplifier stages 1,2 and 3 respectively. We can see the noise from the spectral analyzer is reduced by 5 orders of magnitude in power. In this way the total noise floor can be greatly reduced.

3. Keeping a good connection of ground between instruments will help to reduce ground reference mismatch. Other methods like reducing ground loop area will be discussed later. For any circuit, a proper path for the current to leave from the supply voltage line and return back is critical. The return path is usually selected to be the ground [67]. Ideally, ground potentials of different instruments should be kept the same. But as shown in Figure 4.20 , impedance Z exists along the ground path. When the current flows over, a potential difference will be generated between instruments which leads to an offset. This problem is more obvious at high frequency, when most of the current flow over the surface of conductor due to skin effect, resulting an increase in Alternating Current (AC) impedance [68]. As the current flowing over ground might be alternating, the voltage offset between ground references will vary. This variation of ground reference will add to the signal as a noise source. For all connections we use coaxial cables and additional braided ground straps are used to help lowering down the impedance of the ground connection.

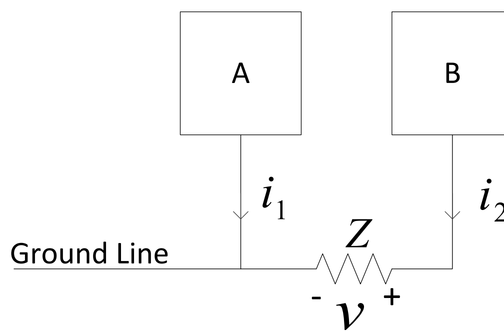


Figure 4.20: Voltage offset in ground between different instruments.

4. Noise from the environment is reduced by shielding, turning off all irrelevant equipments and reducing ground loops. Both the PCB board and the BJT part of circuit are shielded by an aluminum enclosure to reduce the Electromagnetic Interference (EMI) from the environment. Coaxial cables are used for all connections to reduce the influence of EMI to the signal as well reduce the EMI emitted from signals themselves.

We turned off all irrelevant equipments to reduce the emission of EMI. It is also recommended to perform noise measurement at night or weekend when less equipment is being used.

Ground loop is generated when more than one ground path between two instruments exist as shown in Figure 4.21 (a). It will pickup EMI and generate a potential difference on ground reference of different instruments. According to Faraday's Law

$$\oint_L Edl = -\int_S \frac{\partial \Phi}{\partial t} = -\int_S \frac{\partial B}{\partial t} dS \tag{4.35}$$

where E is the electric field, L represents the boundary of the closed area S, Φ is the magnetic flux of area S and B is the magnetic flux density. This equation shows that the integration of the electric field along the boundary of a closed loop equals to the integration of the rate of change of magnetic flux of the area with a reverse direction. As the rate of change of magnetic flux from the environment keeps changing all the time, from a local point of view, the potential difference of ground references will change accordingly. This will introduce fluctuation to the ground reference of equipments and add noise to signal. The equation exhibits that the noise generated from the ground loop can be eliminated by reducing the ground loop area S. Single-point ground connection [69] helps in this way. From Figure 4.21(b) we can see that, instead of connecting the ground of each instrument to the earth ground directly, first connect grounds of instruments together to one point and then connect that point to the building ground will help to reduce the ground loop area. In our test setup, we group all the equipments' power cord to the same power strip before connect them to the building ground.

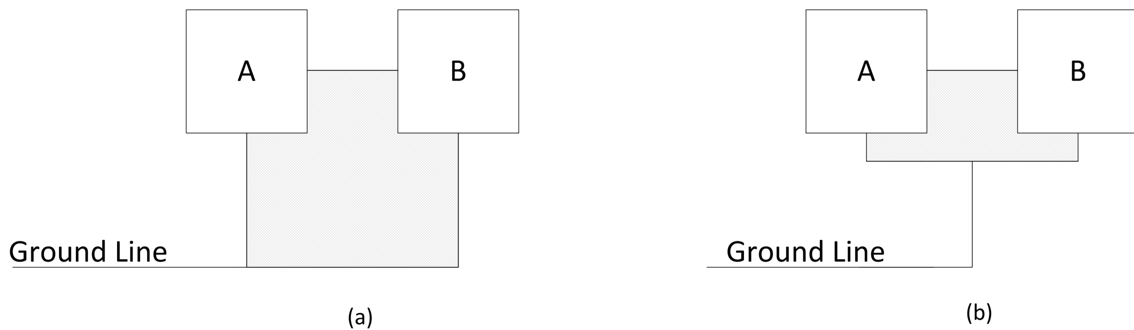


Figure 4.21: (a) Block diagraph shows ground loop. (b) Single point ground connection to reduce the effect of ground loop.

The output of power supplies are insulated from the ground. In this case, by applying the single-point ground strategy we can further reduce the area of the ground loop in the following way. For a power supply, we make it "float" from its own ground. We connect all negative terminals together to the same ground of a particular power supply. This approach can help to reduce the ground loop area formed by power cable as shown in Figure 4.22 $(a), (b)$. The ground loop area can be further reduced by twisting like shown in Figure 4.22(c).

After adopting these methods, the noise floor has been brought down significantly. For the NMOS, our measurement is reliable from 10Hz up to 50MHz as the output noise of DUT is more than one order of magnitude larger than the noise floor. Result is shown in Figure 4.23.

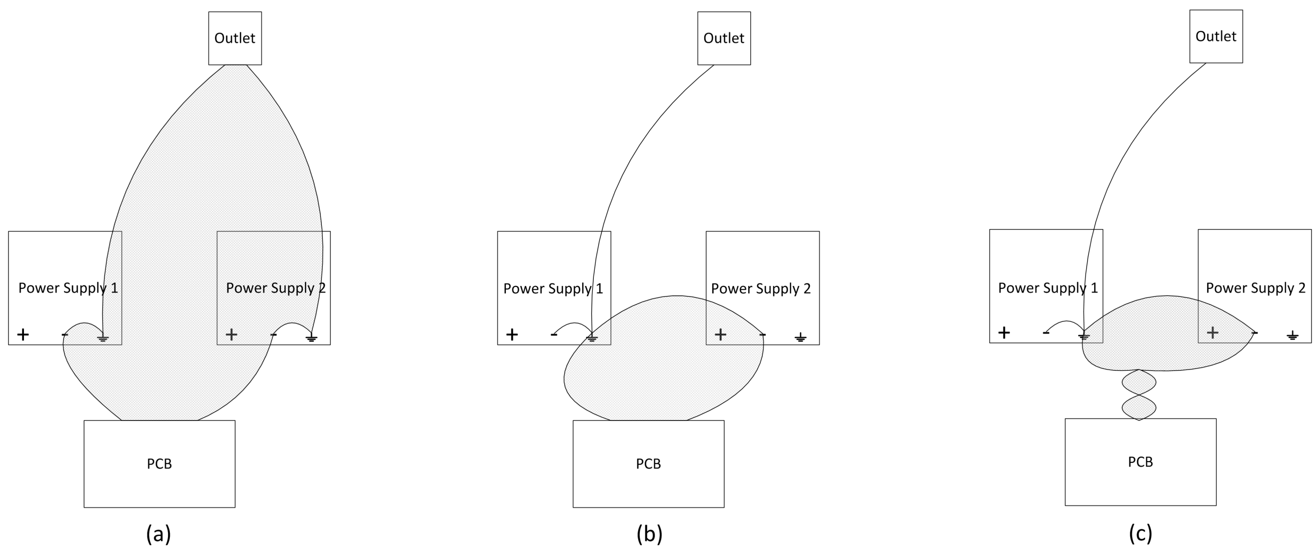


Figure 4.22: (a) Normal connection of power supply. (b) Connect all power supplies' ground to the same one ground point. (c) Twist output of power supply. In all figures, shading area shows the area of ground loop.

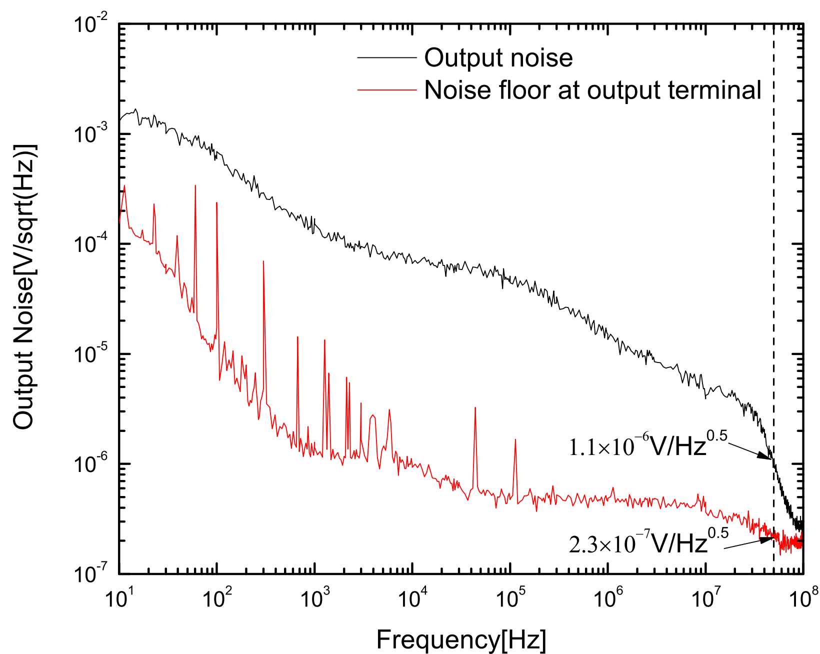


Figure 4.23: Output noise and noise floor at output terminal.

4.3 Noise Degradation Measurement

4.3.1 Measurement result of NMOS

Equivalent input noise measurement before and after hot carrier stress at both 300K and 77K is performed. Let's look at the noise spectrum of fresh devices first. Figure 4.24 (a) illustrates the little temperature dependency of low-frequency noise for NMOS device exists

which agrees well with other results [58, 70]. The little "bump" of the curve at around 1MHz of the device at 77K is a typical Lorentzian Component. It can be explained as additional traps with time constant $\sim 1\mu s$ added on other uniformly distributed traps. Simulation result of the superposition of Lorentzian Component and 1/f spectrum agrees well with the experiment as shown in Figure 4.24 (b). Following the equation 4.7, the expression of Lorentzian Component in the curve we use $\sqrt{S_{vLS,in}} = \sqrt{\frac{2\times10^8}{1\times10^6+1\times\ 10^{-6}(2\pi f)^2}}$. $\sqrt{S_{vf,in}} = 7\times10^{-6}/f^{0.43}$ is used to approximate $1/f$ spectrum.

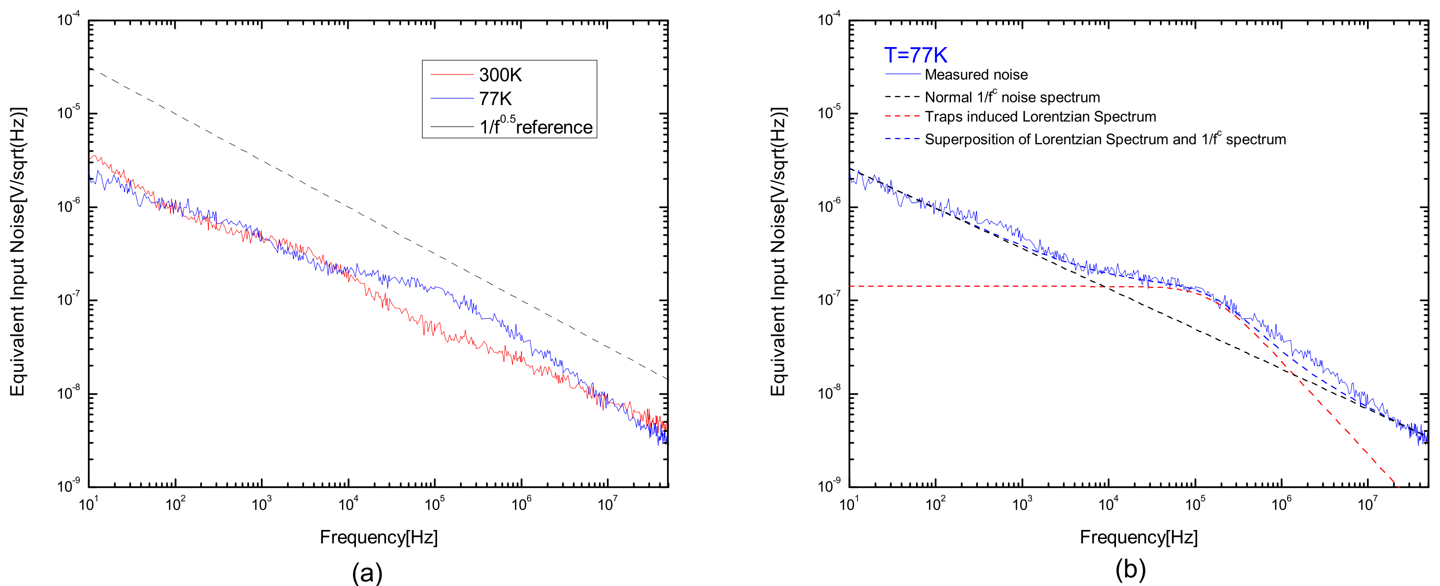


Figure 4.24: (a) Equivalent input noise of fresh NMOS at both 300K and 77K (b) Superposition of Lorentzian Component induced by traps with time constant around 1 μs and a $1/f$ spectrum.

Lorentzian Component may also exist at 300K. Figure 4.25 exhibits the noise spectrum of two fresh NMOS in same parameter at 300K. Device 1 shows a Lorentzian Component.

Noise measurements before and after degradation of NMOS are shown in Figure 4.26. Similar to reports from literature [15], we can see the obvious increase of low-frequency noise at both 300K and 77K.

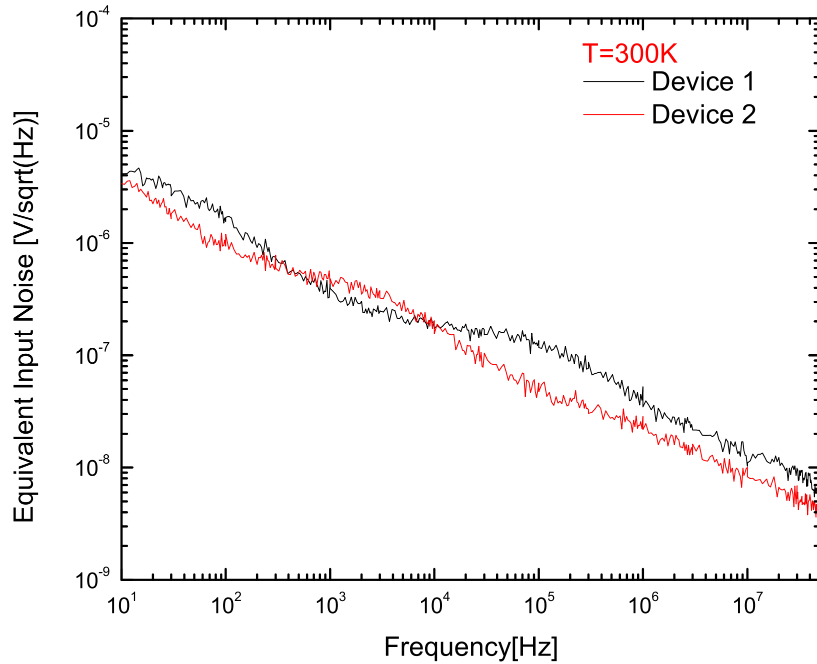
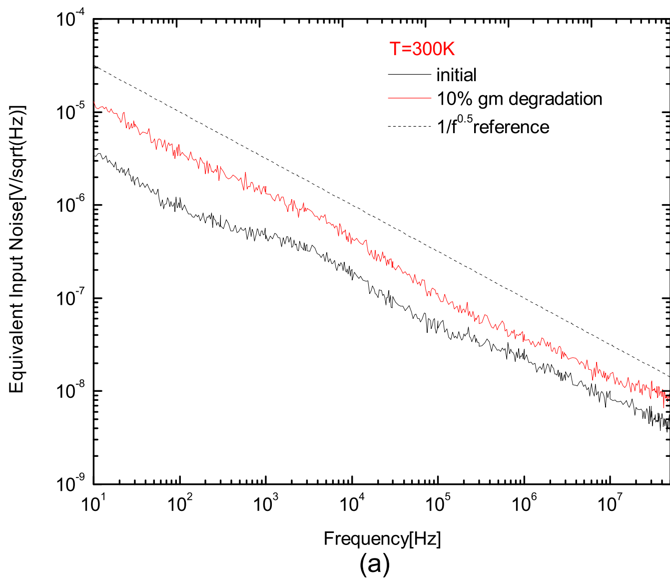


Figure 4.25: Noise of two fresh NMOS devices measured at 300K.



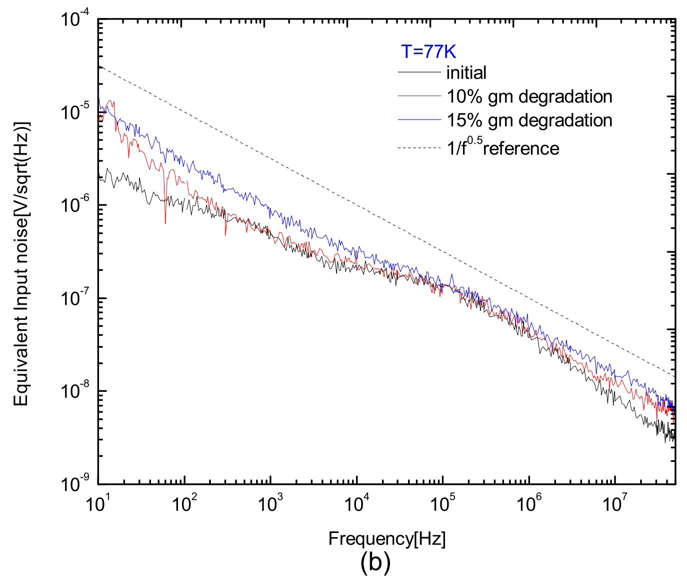
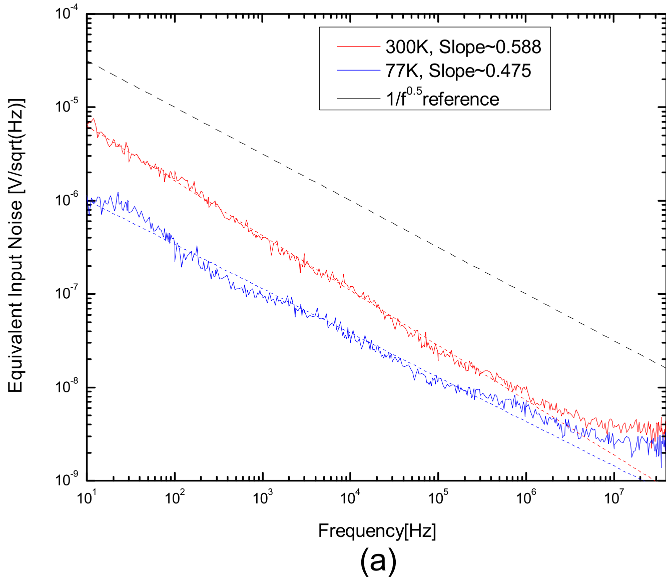


Figure 4.26: Equivalent input noise of NMOS degradation at $(a)300K$ and $(b)77K$.

4.3.2 Measurement result of PMOS

The equivalent input noise of fresh PMOS device at both 300K and 77K is shown in Figure 4.27 (a). Low-frequency noise at 77K is about 2 orders of magnitude lower than that at 300K in power. The slope of low-frequency noise is smaller at 77K (the factor AF in the Equation 4.8 changes from 1.176 at 300K to 0.95 at 77K). Similar temperature dependency can also be found in the literature [71]. PMOS is believed to be at least one order of magnitude lower (in power) than NMOS in the same size and process [21] which is demonstrated in Figure 4.27(b).



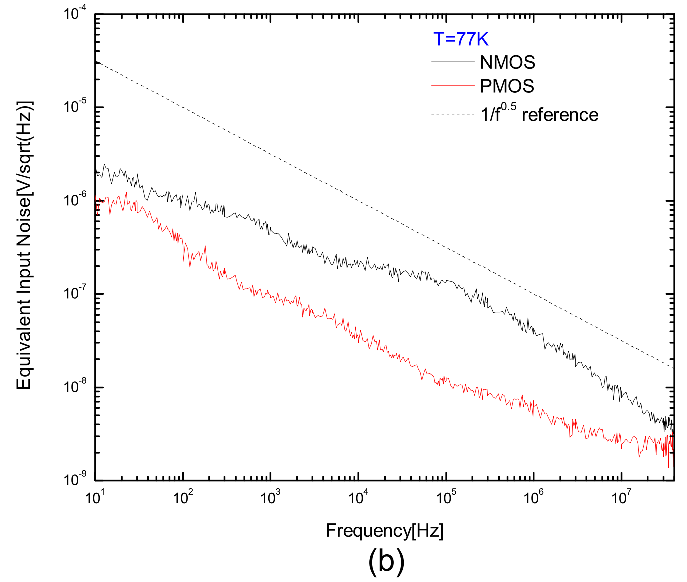
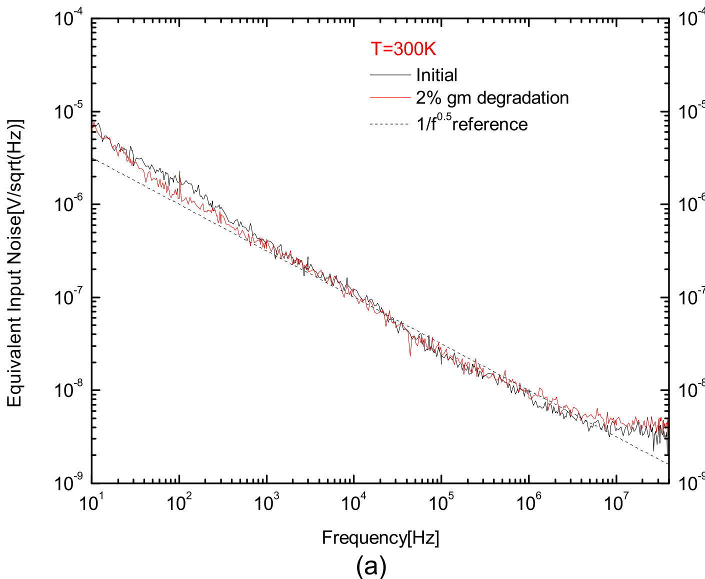


Figure 4.27: (a) Noise spectrum of PMOS at 300K and 77K. (b) Noise comparison of NMOS and PMOS at 77K.

PMOS is also believed to be more resistive to the low-frequency noise degradation due to hot carrier injection [72]. For PMOS, we call the device is degraded when transconductance reaches 2% degradation which already requires a much longer stressing time than 10% degradation in transconductance of NMOS. From Figure 4.28 we can see that the stress has little influence on low-frequency noise in PMOS.



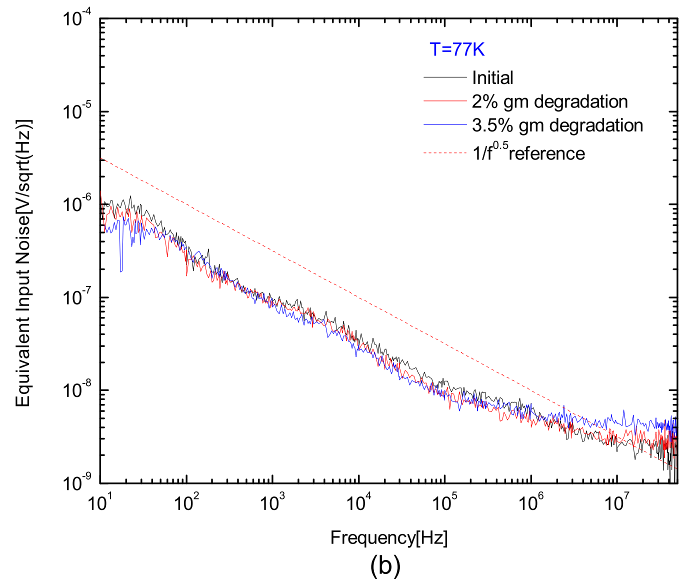


Figure 4.28: Equivalent input noise of PMOS degradation at $(a)300K$ and $(b)77K$.

Due to the lower low-frequency noise at 77K, the higher tolerance to noise degradation during HCE and the longer lifetime, PMOS is chosen as the input MOSFET in the preamplifier which is the dominant noise contributor in the front-end ASIC [9]. To suppress the

impact of hot carrier degradation on noise even further, the input PMOS transistor is designed to operate at $V_{ds} \sim 200mV$, where hot carrier effects is negligible. The much larger transconductance degradation in NMOS transistors is accompanied by an increase of low-frequency noise. The effect of this on the ASIC overall noise is made negligible by $a)$ the circuit design minimizing the later stage noise contributions, and altogether by $b)$ the circuit design avoiding stress conditions.

Chapter 5

Conclusion

A study of hot-carrier effects on TSMC 180nm CMOS device lifetime has been performed at 300K and 77K, with an intended application for LAr TPC readout in LBNE. Two different measurement strategies are adopted: accelerated lifetime measurement under severe electric field stress by large V_{ds} while observing degradation in the transistor transconductance, and a separate measurement of the substrate current density as a function of $1/V_{ds}$ before and after the stress test. The canonical very steep slope of the inverse relation between the lifetime and the substrate current density is verified at 77K. PMOS exhibits a much longer lifetime than NMOS during HCE at both 300K and 77K. Degradation of MOSFETs' characteristics(transconductance, threshold voltage and subthreshold swing) due to HCE are also investigated theoretically and experimentally. The study confirms that below a certain value of V_{ds} a lifetime margin of several orders of magnitude can be achieved for the cold electronics TPC readout at 77K.

The degradation of MOSFET noise due to HCE is studied at both 300K and 77K. The mechanism of low-frequency noise and its relationship with HCE are discussed. A noise spectrum measurement system operates from 77K to 300K is designed. Approaches adopted to achieve low noise floor of the measurement system are introduced. Measurements illustrate that PMOS exhibits a lower noise level as well as more resistant to HCE than NMOS. Little influence of HCE on low-frequency noise of PMOS can be observed makes it a good candidate as the input transistor of the pre-amplifier in the front-end ASIC which is a major noise contributor of the system.

This lifetime study has helped us to establish confidence about lifetime and performance of the CMOS front-end ASIC to be operated in LAr. The study makes it possible for us to extrapolate the design criteria for the front-end electronics at cryogenic temperature with a long lifetime:

- Lifetime scales inversely with the drain current density. Operation of transistors in moderate inversion results in long lifetime.
- According to Equation 2.27
$$\tau = C_3 \frac{W}{I_{ds}} e^{\varphi_{it}/q\lambda E_m} \tag{5.1}$$
the apparent larger degradation of transistor at cryogenic temperature can be avoided by keeping the term λE_m the same as at RT which can be achieved by

- Reducing the maximum V_{ds} by 7 to 10%
- Increasing the minimum length of the transistor (e.g., by 50%)

- PMOS is more robust towards HCE, confirmed by lower-frequency noise degradation. It is suggested to be used as the input transistor of the preamplifier, which is the main noise contributor in front-end ASICs.

With the proposed design guideline, the front-end ASIC in LAr TPC is designed for long lifetime operation as well as low noise degradation. Long lifetime is ensured by avoiding stress condition with $V_{ds} < 1.6V$. Low noise degradation is reached by utilizing PMOS as input MOSFET in the preamplifier and operate at $|V_{ds}| \sim 200mV$ where HCE should be eligible. The effect of larger noise degradation of NMOS is relieved by reducing the noise contribution from NMOS to the fron-end ASIC during circuit design.

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